Machakos University College

(A Constituent College of Kenyatta University)

UNIVERSITY EXAMINATIONS 2014/2015

SCHOOL OF ENGINEERING AND TECHNOLOGY

FIRST SEMESTER EXAMINATIONS FOR THE DEGREE OF BACHELOR OF SCIENCE IN COMPUTER SCIENCE

SCO 106: ELECTRONICS

DATE: 15/12/2014 **TIME: 8.30 a. m. – 10.30 a. m.**

INSTRUCTIONS: *Answer **QUESTION ONE** and **ANY** other **TWO** questions.*

QUESTION ONE (COMPULSORY): 30 MARKS

a. A certain conducting wire has an electrical resistance of 20 Ω at 12 °C and at 25 °C the resistance increases to 30 Ω. Determine the temperature coefficient of resistance for the metal of which the conductor is made. (4 Marks)

b. Draw the general scheme for a state machine. (4 Marks)

c. Prove that $ABCD + AB\overline{C}\,\overline{D} + ABC\overline{D} + AB\overline{C}D + ABCDE + AB\overline{C}\,\overline{D}\,\overline{E} + AB\overline{C}DE$ can be simplified to AB. (5 Marks)

d. Use diagrams to illustrate the simplified models and circuit symbols of npn and pnp BJTs. (4 Marks)

e. Sketch the test circuit diagram representing a circuit that can be used to obtain the forward characteristic of a small-signal silicon diode. (3 Marks)

f. A transistor operates with a collector current of 98 mA and an emitter current of 100 mA. Determine the value of the base current and the common emitter current gain. (4 Marks)

g. Draw the circuit symbols for the three most basic logic gates and present their respective Boolean expressions and truth tables. (6 Marks)

QUESTION TWO: 20 MARKS

a. Implement the POSs Boolean function expressed by ∏1, 2, 5 using a suitable multiplexer. (12 Marks)

b. Implement a full adder circuit using a 3-to-8 line decoder. (8 Marks)

QUESTION THREE: 20 MARKS

a. Draw circuit symbols of the following logic gates: NAND, NOR, Ex-OR, Ex-NOR and present their corresponding Boolean equations and truth tables. (8 Marks)

b. Illustrate how to hardware implement the following:

i. A four-input NAND gate using two-input AND gates and NOT gates.

ii. A three-input NAND gate using a two-input NAND gate.

iii. A NOT circuit using a two-input NAND gate.

iv. A NOT circuit using a two-input NOR gate.

v. A NOT circuit using a two-input EX-OR gate. (12 Marks)

QUESTION FOUR: 20 MARKS

a. i. Distinguish between a combinational logic circuit and a sequential logic circuit.

ii. Draw the block diagram of a generalized combinational circuit. (5 Marks)

b. State the seven different steps involved in the design of a combinational logic circuit. (7 Marks)

c. By considering relevant Boolean expressions for half-adder and half-subtractor circuits, design a half-adder-subtractor circuit that can be used to perform either addition or subtraction on two one-bit numbers in such a way that the desired arithmetic operation is selectable from a control input. (8 Marks)