MACHAKOS UNIVERSITY

University Examinations for 2017/2018

SCHOOL OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF COMPUTING AND INFORMATION TECHNOLOGY

THIRD YEAR SECOND SEMESTER EXAMINATION FOR BACHELOR OF INFORMATION TECHNOLOGY

ACU SIT 311: COMPUTER ARCHITECTURE

DATE: 15/12/2017   **TIME: 2.00-4.00 PM**

INSTRUCTIONS

Answer question **ONE** and **Any** other **Two** among the four selective questions

QUESTION ONE (COMPULSORY) (30 MARKS)

a)   Define interrupt   (2 marks)

b)   Describe multiple and single implementations of bus syatems.   (6 marks)

c)   Using a well labelled diagram, explain organization of a memory   (7 marks)

d)   By use of diagrams, describe the structure of Von Neuman Computer   (6 marks)

e)   Describe any three types of addressing modes including an example in each.   (9 marks)

QUESTION TWO (20 MARKS)

a)   Explain any three mapping procedures in the organization of cache memory with the use of example.   (9 marks)

b)   Contrast RISC and CISC   (5 marks)

c)   Describe the following instruction cycles using instruction cycle diagram   (6 marks)

         i.   Fetch/execute

         ii.   Interrupt driven

QUESTION THREE (20 MARKS)

a)   Explain how ALU will perform the following arithmetic 30_{10}-42_{10} (6 marks)

b)   Describe memory hierarchy indicating clearly the kind of data transferred between each level   (8 marks)

c)   Explain the following mechanisms for I/O transfer   (6 marks)

      i.   Program-controlled I/O

      ii.   Direct Memory Access

QUESTION FOUR (20 MARKS)

a)   Using a block diagram of a complete processor, explain the organization of a processor

                                                                                                            (6 marks)

b)   Explain the concept of virtual memory and show how virtual address is mapped to actual physical address.   (8 marks)

c)   Describe instruction pipeline   (6 marks)

QUESTION FIVE (20 MARKS)

a)   Evaluate (A+B) * (C+D) using the following address machines.   (9 marks)

      i.   Two Address Machine

      ii.   Three Address Machine

      iii.   One Address Machine

b)   Differentiate PCI and SCSI buses   (5 marks)

c)   For the following memory units (specified by the number of words the number of bits per word), determine the number of address lines, input/output lines and the number of bytes that can be stored in the specified memory   (6 marks)

      i.   64K x 8

      ii.   4G x 64