MACHAKOS UNIVERSITY COLLEGE

(A Constituent College of Kenyatta University)
University Examinations for 2015/2016 Academic Year

SCHOOL OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

SECOND SEMESTER EXAMINATION FOR DIPLOMA IN ELECTRIC AND ELECTRONICS ENGINEERING

EED 316: DATA COMMUNICATION

DATE: **TIME:**

INSTRUCTIONS

Answer Question ONE And Any Other Two Questions From Section B

SECTION A: (COMPULSORY)

1. a) Explain any five components of data communication. (10 marks)

   b) With the aid of a block diagram, show the data communication system. (10 marks)

   c) Explain any four different forms in which data can be represented. (8 marks)

   d) What is the maximum data rate for a 3 kHz channel that transmits data using 2 levels? (2 marks)

SECTION B: ANSWER ANY OTHER TWO QUESTIONS

2. a) i) Explain any three reasons for choosing encoding techniques in data communication. (9 marks)

   ii) A complex low-pass signal has a bandwidth of 200 kHz. What is the minimum sampling rate for this signal? (6 marks)

   b) List Factors that are used to Compare Encoding Schemes in data communication. (5 marks)

3. a) With the aid of a block diagram show how the components of a pulse code modulation (PCM) encoder, modulates an analogue signal to a digital signal. (10 marks)

b) Using sinusoidal wave signals, illustrate aliasing sampling technique. (4 marks)

c) Highlight the differences between the following modes of communication
   i) Simplex
   ii) Half-duplex
   iii) Full-duplex (6 marks)

4. a) Using 11001011001010101 digital bits, illustrate the following digital signals
   i) Unipolar encoding
   ii) Non-return to zero NRZ
   iii) Non-return to zero NRZ-I
   iv) Manchester (10 marks)

b) With the aid of the use of diagrams, illustrate the following bipolar encoding techniques
   i) Amplitude shift keying (ASK)
   ii) Frequency shift keying (FSK)
   iii) Phase shift keying (PSK) (10 marks)

5. a) Compare datagram packet switching with virtual circuit packet switching. (10 marks)

b) Draw example timing diagrams to show how a Stop-and-wait ARQ scheme copes with:
   1. A damaged data frame;
   2. A lost data frame;
   3. A lost ACK. (10 marks)