MACHAKOS UNIVERSITY

University Examinations for 2018/2019

SCHOOL OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF COMPUTING AND INFORMATION TECHNOLOGY

THIRD YEAR SECOND SEMESTER EXAMINATION FOR

BACHELOR OF SCIENCE (INFORMATION TECHNOLOGY)

SIT311: COMPUTER ARCHITECTURE

DATE: 24/4/2019 **TIME: 8.30-10.30 AM**

INSTRUCTIONS

Answer **question ONE and any other TWO questions.**

QUESTION ONE (30 MARKS)

a) With aid of a diagram explain the components of von Neumann computer architecture (6 marks)

b) Define the following terms as used in computer architecture (8 marks)

i. Instruction Set Architecture

ii. Cache memory

iii. Branch instruction

iv. Interrupt

c) Differentiate between immediate and register addressing modes (4 marks)

d) Briefly explain CPU instruction execution cycle (6 marks)

e) The table below shows frequency of all instruction types executed in a typical program, and the number of cycles per instruction for each type. Compute the CPI metric (4 marks)

Instruction Type	Frequency	Cycles
ALU Instruction	50%	4
Load Instruction	30%	5
Store Instruction	5%	4
Branch Instruction	15%	2

f) Find the two's complement representation of -43_{10} (2 marks)

QUESTION TWO (20 MARKS)

a) Describe the computer memory hierarchy (8 marks)

b) Explain the following types of Cache memory mapping (9 marks)

i. Direct mapping

ii. Set associative mapping

iii. Fully Set Associative mapping

c) State any THREE elements of an instruction (3 marks)

QUESTION THREE (20 MARKS)

a) Explain the difference between Hardwired and Micro-Programed Control Units (6 marks)

b) Explain the functions of the following CPU registers (8 marks)

i. Accumulator

ii. Instruction register (IR)

iii. Memory Address Register (MAR)

iv. Program Counter (PC)

c) Distinguish between Reduced Instruction Set Architecture (RISC) and Complex Instruction Set Architecture (CISC) (6 marks)

QUESTION FOUR (20 MARKS)

a) Suppose a program task takes 2 million instructions to execute on a processor running at 2 GHz. Suppose also that 50% of the instructions execute in 3 clock cycles, 40% execute in 4 clock cycles, and 10% execute in 5 clock cycles. What is the execution time for the task? (6 marks)

b) Suppose the processor described in *part a of Question Four* above is redesigned so that all instructions that initially executed in 4 cycles now execute in 3 cycles and the clock rate is decreased from 2.0 GHz to 1.9 GHz. If no changes to the instruction set, find the percentage improvement in performance. (4 marks)

c) With aid of diagrams explain the following addressing modes (6 marks)

i. Stack addressing mode

ii. Displacement addressing mode

d) Differentiate between Level 1(L1) and Level 2 (L2) cache memory (4 marks)

QUESTION FIVE (20 MARKS)

a) The CPU time metric is defined as the ratio of the *clock cycles for a program to the clock rate.* Explain three ways in which CPU time can be decreased (6 marks)

b) Convert each of the following into binary (6 marks)

a. 2.25

b. -5.75

c) Explain the following methods of computer memory access (6 marks)

i. Sequential

ii. Random

iii. Direct

d) State 2 disadvantages of assembly programming (2 marks)