



MACHAKOS UNIVERSITY

University Examinations for 2019/2020 Academic Year

SCHOOL OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

SECOND YEAR SECOND SEMESTER EXAMINATION FOR

BACHELOR OF SCIENCE (TELECOMMUNICATION AND INFORMATION
TECHNOLOGY)

SPH 207: DIGITAL ELECTRONICS AND DEVICES

DATE: 24/11/2020

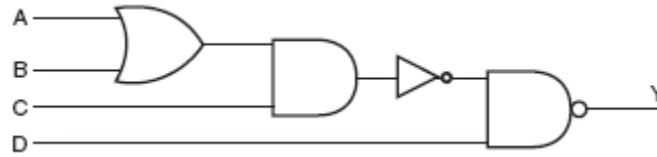
TIME: 8.30-10.30 AM

INSTRUCTIONS

Answer Question One and Any Other Two Questions

QUESTION ONE (30 MARKS)

- a) Briefly describe the following flip-flop timing parameters:
- i. Set-up time and hold time;
 - ii. Propagation delay;
 - iii. Maximum clock frequency. (6 marks)
- b) i Differentiate between decimal number system and hexadecimal number system hence convert $A031_{16}$ to its decimal equivalent. (5 marks)
- ii Simplify the following algebraic expression and use a logic gate for its implementation.
 $BC'D' + A'BD + ABD + BCD' + B'CD + A'B'C'D + AB'C'D.$ (5 marks)
- iii Draw the truth table of the logic circuit shown in below.



(6 marks)

- iv It is proposed to construct an eight-input NAND gate using only two-input AND gates and two-input NAND gates. Draw the logic arrangement that uses the minimum number of logic gates. (8 marks)

QUESTION TWO (20 MARKS)

A factory crane operator is to control a RED and GREEN lights by four switches. A, B, C and D. Design a simple logic system which will operate under the following conditions

- a) RED light is ON for
 - i. Switch A on, switch B off, OR
 - ii. Switch C on.
- b) GREEN light ON for
 - i. Switches A and B on AND
 - ii. Switches C and D off. (10 marks)
- c) using k map simplify the below expression to its simplest form (10 marks)

$$Y = A'B'C' + A'BC' + AB'C' + AB'C + ABC' = ABC$$

QUESTION THREE (20 MARKS)

- a) With the help of the logic diagram, describe the operation of a clocked R-S flip-flop with active LOW R and S inputs. (10 marks)
- b) Explain the meaning of the terms
 - i. Noise immunity
 - ii. Fan out
 - iii. Modulus of a counter (6 marks)
- c) Describe any two logic families (4 marks)

QUESTION FOUR (20 MARKS)

- a) Briefly describe the operational aspects of bistable, monostable and astable multivibrators. (6 marks)
- b) Design a modulo-5 asynchronous counter using a J-K negative going edge triggered flip flops (10 marks)
- c) Explain two differences of CMOS logic compared to NMOS (4 marks)

QUESTION FIVE (20 MARKS)

- a) Identify two main components of a typical data acquisition system. (2 marks)
- b) Give the logic families that are most suitable for applications that requires
 - i. High speed
 - ii. Low power
 - iii. High noise immunity. (3 marks)
- c) Describe the improvements that a J-K flip flop have over a clocked R-S flip-flop with the help of appropriate diagrams. (6 marks)
- d) Convert the following to their corresponding equivalence
 - i. 2479 to its corresponding hexadecimal equivalent
 - ii. 11010_2 to its corresponding decimal equivalent
 - iii. 0.85 to its binary equivalent (9 marks)