MACHAKOS UNIVERSITY

University Examinations for 2019/2020Academic Year

SCHOOL OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

FIFTH YEAR SECOND SEMESTER EXAMINATION FOR

BACHELOR OF SCIENCE IN ELECTRICAL AND ELECTRONICS ENGINEERING

EEE 533: ELECTRONIC CIRCUITS AND SYSTEMS

DATE: 22/10/2020 **TIME: 8.30-10.302 AM**

INSTRUCTIONS

Answer Question One and Any Other Two Questions

QUESTION ONE (30 MARKS)

a) Consider the circuit in Fig.Q1 (a). Neglect base currents and assume $V_A = \infty$.

i. Derive the expression for I_O in terms of I_{REF} and R_E.

ii. Determine the value of R_E such that $I_O = I_{REF} = 100\ \mu A$. Assume $V_{BE} = 0.7V$ at a collector current of 1 mA.

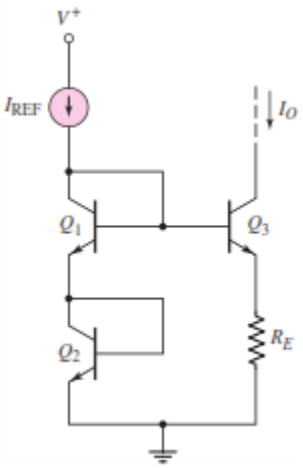

Fig.Q1 (a) (9 marks)

b) The MOSFET current-source circuit in Fig.Q1 (b) is biased at $V^+ = 2.0$ V. The transistor parameters are $V_{TN} = 0.5$ V, $k'_n = 80\ \mu A/V^2$, and $\lambda = 0.015\ V^{-1}$.

i. Design the circuit such that $I_{REF} = 50\ \mu A$ and the nominal bias current is $I_O = 100\ \mu A$.

ii. Find the output resistance R_o;

iii. Determine the percentage change in I_o for a change in drain-to-source voltage of $\Delta V_{DS2} = 1$ V.

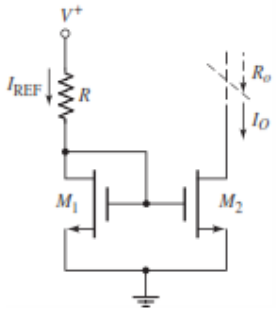

Fig.Q1(b). (9 marks)

c) The control line of a VCO senses a rectangular signal toggling between $V_1$and V_2 at a period T_m. Plot the frequency, phase, and output waveform as a function of time. (8 marks)

d) Describe any two problems of a simple modulator. (4 marks)

QUESTION TWO (20 MARKS)

a) A VCO senses a small sinusoidal control voltage $V_{cont} = V_m \cos \omega_m t$. Determine the output waveform and its spectrum. (12 marks)

b) In Fig. Q2 (b), $R_1$and $R2$ are equal and sustain equal voltages, each carrying a current of $(V_T \ln n)/R_3$. We therefore have

$V_{out} = V_{BE1} + (V_T \ln n)R_1/R_3$

But the second term is *not* equal to $17.2V_T$ if we have already chosen $(V_T \ln n)(1 + R_2/R_3) = 17.2V_T$. Explain this discrepancy.

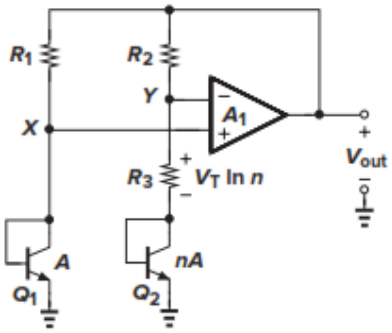

Fig.Q2 (b) (8 marks)

QUESTION THREE (20 MARKS)

a) Implement a simple PLL in CMOS technology. (4 marks)

b) Explain the following terms with respect to phase locked loops (PLLs) application:

i. Frequency synthesis;

ii. Skew reduction;

iii. Jitter reduction. (6 marks)

c) A cellular telephone incorporates a 900-MHz phase-locked loop to generate the carrier frequencies. If $\omega_{LPF} = 2\pi \times$ (20 kHz) and the output frequency is to be changed from 901 MHz to 901.2 MHz, how long does the PLL output frequency take to settle within 100 Hz of its final value? (5 marks)

d) Suppose a type I PLL experiences a frequency step$\Delta\omega$ at $t = 0$. Calculate the change in the phase error (5 marks)

QUESTION FOUR (20 MARKS)

a) Consider a 3-bit D/A converter in which V_{ref} = 4V, with the following measured voltage values:

{0.011: 0.507: 1.002: 1.5011: 1.996: 2.495: 2.996: 3.491}

i. Find the offset and gain errors in units of LSBs;

ii. Find the INL (endpoint) and DNL errors (in units of LSBs);

iii. Find the effective number of bits of absolute accuracy;

iv. Find the effective number of bits of relative accuracy. (14 marks)

b) i An 8-bit D/A converter has $V_{ref} = 5$ V. What is the output voltage when $B_{in} =$ 10110100?

ii. Find V_{LSB}. (6 marks)

QUESTION FIVE (20 MARKS)

a) With the aid of a block diagram describe the operation of a logic analyzer. (10 marks)

b) With the aid of a circuit diagram describe the operation of a 4 bit R-2R based DAC. (10 marks)