MACHAKOS UNIVERSITY

University Examinations for 2021/2022

SCHOOL OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

SECOND YEAR SECOND SEMESTER EXAMINATION FOR

BACHELOR OF SCIENCE (TELECOMMUNICATION AND INFORMATION TECHNOLOGY)

SPH 207: DIGITAL ELECTRONICS AND DEVICES

DATE: 15/12/2021 **TIME: 8.30-10.30 AM**

INSTRUCTIONS:

Answer Question One And Any Other Two Questions

QUESTION ONE (COMPULSORY) (30 MARKS)

a) It is proposed to construct an eight-input NAND gate using only two-input AND gates and two-input NAND gates. Draw the logic arrangement that uses the minimum number of logic gates. (5 marks)

b) Briefly describe the operational aspects of bistable, monostable and astable multivibrators with their corresponding timing diagrams (9 marks)

c) Simplify the following Boolean functions

(i) AB'+A'B+AB+A'B

(ii) A[B+C(AB+AC)] (6 marks)

d) Describe the following

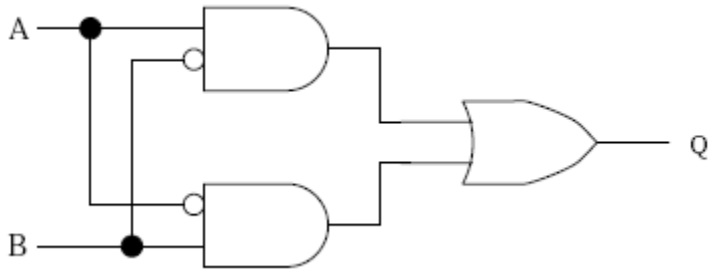
(i) Logic gate propagation delay

(ii) Set-up time and hold time

(iii) Maximum clock frequency (6 marks)

(iv)

e) Draw the truth table of the logic circuit shown in below



(4 marks)

QUESTION TWO (20 MARKS)

Show how a power sourse, a lamp and a number of switches can be used to represent the following logical functions.

a) L=A.B.C

b) L=A+B+C

c) L=(A.B)+(C.D)

d) L=A+B (10 marks)

QUESTIONTHREE (20 MARKS)

Convert the following hexadecimal numbers to binary and octal:

a) EF69, 98AB5 (4 marks)

b) Compare the standard TTL, low-power Schottky TTL and Schottky TTL on the basis of speed, power dissipation and fan-out capability (6 marks)

c) With the help of the logic diagram, describe the operation of a clocked R-S flip-flop with active LOW R and S inputs. (10 marks)

QUESTION FOUR (20 MARKS)

a) Design a decade ripple counter using a J-K negative going edge triggerd flip flops (10 marks)

b)

Calculate $A + B$, $A - B$, $A \times B$, and $A \div B$ for the following pairs of binary numbers.

(a) 10101, 1011

(b) 1011010, 101111

(c) 101, 1011

(10 marks)

QUESTION FIVE (20 MARKS)

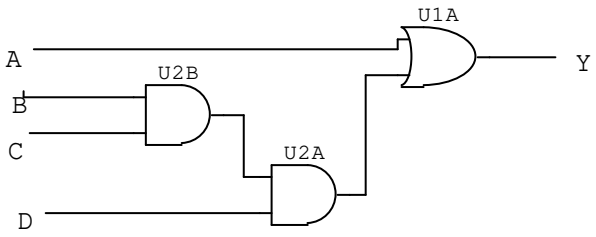
(a) Explain threee advantages of CMOS logic compared to NMOS , stating which logic families that are most suitable for applications that requires

(i) High speed

(ii) low power consuption

(iii) high noice immunity (6 marks)

(b) Find the boolean expression for the out put of fig below and compute the output value when A=0, B=1, C=0 and D=1



(4 marks)

(c) From the truth table below,derive

(i) logic expression for F

(ii) simplify the expression as far as possible

(iii) draw the logic diagram to imlement this (10 marks)

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1