MACHAKOS UNIVERSITY

University Examinations for 2023/2024 Academic Year

SCHOOL OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

THIRD YEAR ……..SEMESTER EXAMINATION FOR

BACHELOR OF SCIENCE (TELECOMMUNICATION AND INFORMATION TECHNOLOGY)

SPH312: COMPUTER ARCHITECTURE & ORGANIZATION

DATE: **TIME:**

INSTRUCTIONS

Answer Question One and Any Other Two Questions

QUESTION ONE(COMPULSORY) (30 MARKS)

a) Differentiate computer architecture and computer organization. (4 marks)

b) Simplify the following expression using the Boolean theorems/laws and hence verify the results by using Karnaugh maps (5 marks)

$$F = \bar{x}yz + \bar{x}y\bar{z} + xz$$

c) Of all the three representations viz., Signed magnitude, Signed 1's complement and Signed 2's complement determine the representation that is widely used in the digital computers giving reasons for the same. (3 marks)

d) Perform the following operations (A) + (B) and (A) – (B) for an 8 bit number (one bit for sign and seven bits for magnitude) using 2's complement. (6 marks)

e) Use a suitable diagram to explain the concept of cache memory. (6 marks)

f) The block diagram in Figure Q1 (f) represents a state machine. Considering the state machine's components and the digital values present on each of the connections, determine:

i. The maximum number of states this system could have

ii. The number of rows are in the truth table defining the output

iii. The number of rows are in the truth table defining the next state

iv. The current state of this system

v. The next state if the clock were to pulse right now. (6 marks)

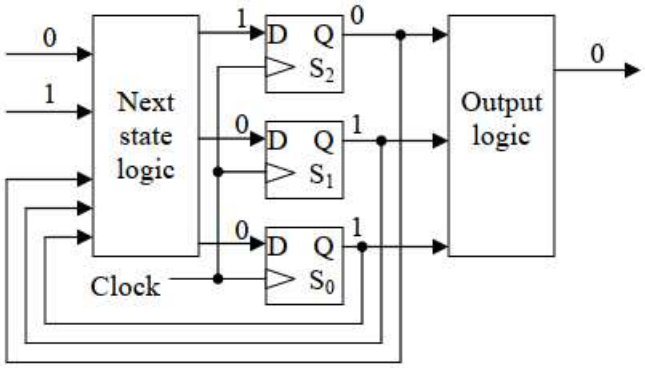

Figure Q1 (f)

QUESTION TWO (20 MARKS)

a) Explain the difference between combinational circuits and sequential circuits. (2 marks)

b) When a CPU is PERFORMING let say arithmetic operations, the operands can come from different locations within the CPU. Design a simple two way device that will select the inputs to the operation from the possible locations. (6 marks)

c) From the truth table for two bit addition with carry input, design a full adder circuit using two half adder circuits. (12 marks)

QUESTION THREE (20 MARKS)

Design a counter that has an $Enable$ input. When $Enable = 1$, it increments through the sequence $0, 1, 2, 3, 0, 1, \ldots,$ incrementing each clock tick. $Enable = 0$ causes the counter to remain in its current state. The output is the sequence number in two-bit binary. Show all your workings. (20 marks)

QUESTION FOUR (20 MARKS)

a) Explain why refreshing is required in Dynamic RAM. (3 marks)

b) Explain how a RAM of capacity 2 K bytes can be mapped into the address space 1000_H to $17FF_H$ of a CPU having a 16 bit address lines. Show how the address lines are decoded to generate the chip select condition for the RAM. (8 marks)

c) Determine the number of 256×4 RAM chips needed to provide a memory capacity of 2048 bytes. Show also the corresponding interconnection diagram. (9 marks)

QUESTION FIVE (20 MARKS)

a) Define the following terms:

i. Instruction cycle

ii. Machine cycle

iii. T – states (5 marks)

b) Explain THREE main advantages of general-register based CPU organizations over stack based CPU organizations. (6 marks)

c) Describe the general structure of a central processing unit (CPU) using a block diagram. (9 marks)