MACHAKOS UNIVERSITY

University Examinations for 2019/2020Academic Year

SCHOOL OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

THIRD YEAR SECOND SEMESTER EXAMINATION FOR

BACHELOR OF SCIENCE IN ELECTRICAL AND ELECTRONICS ENGINEERING

EEE 306: DIGITAL ELECTRONICS II

DATE: 23/11/2020 **TIME: 2.00-4.00 PM**

INSTRUCTIONS

Answer Question One and Any Other Two Questions

QUESTION ONE (30 MARKS)

a) Distinguish between synchronous and asynchronous counters. (3 marks)

b) Draw the circuit diagram of a 4-bit ripple counter using JK flip flops. (3 marks)

c) Explain the addition process using both half adder and full adder circuits (use truth tables). Draw the resulting adder circuits from the two addition processes. (7 marks)

d) Show the implementation of the following Boolean function using:

(i) 16×1 Multiplexer and

(ii) 8×1 multiplexers (6 marks)

$$F = \Sigma(1,3,4,11,12,13,14,15)$$

e) Design a 3 bit counter which counts in the sequence: 001, 011, 010, 110, 111, 101, 001 using D flip flops. Do not use a decoder in you design. (7 marks)

f) Draw the gate-level circuit diagram of a three-to-eight line decoder and explain its working using a truth table. (4 marks)

QUESTION TWO (20 MARKS)

a) Design a 3-bit synchronous binary counter using T flip-flops. (7 marks)

b) The even parity function has the truth table shown below. Implement this parity function using a 4*1 Multiplexer (4 marks)

A	B	C	F_1
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

c) Implement the full adder using a decoder and external OR gates. (5 marks)

d) Draw the PLA circuit that implements the following functions (4 marks)

$$F_0 = A\overline{B} + \overline{A}B + \overline{A}\,\overline{B}$$

$$F_1 = A\overline{B} + \overline{A}B + AB$$

QUESTION THREE (20 MARKS)

a) Show the gate level implementation of a 4*1 multiplexer. (4 marks)

b) Design a 3-bit Gray code counter using JK flip-flops. (7 marks)

c) Construct a 4 × 16 decoder can be constructed using two 3 × 8 decoders. (4 marks)

d) A 10-bit digital slope integrating A/D converter has a full-scale input of 10V. If the clock period is 15 μS, how long will it take to convert an input of 4V? How long for an input of 10V? (5 marks)

QUESTION FOUR (20 MARKS)

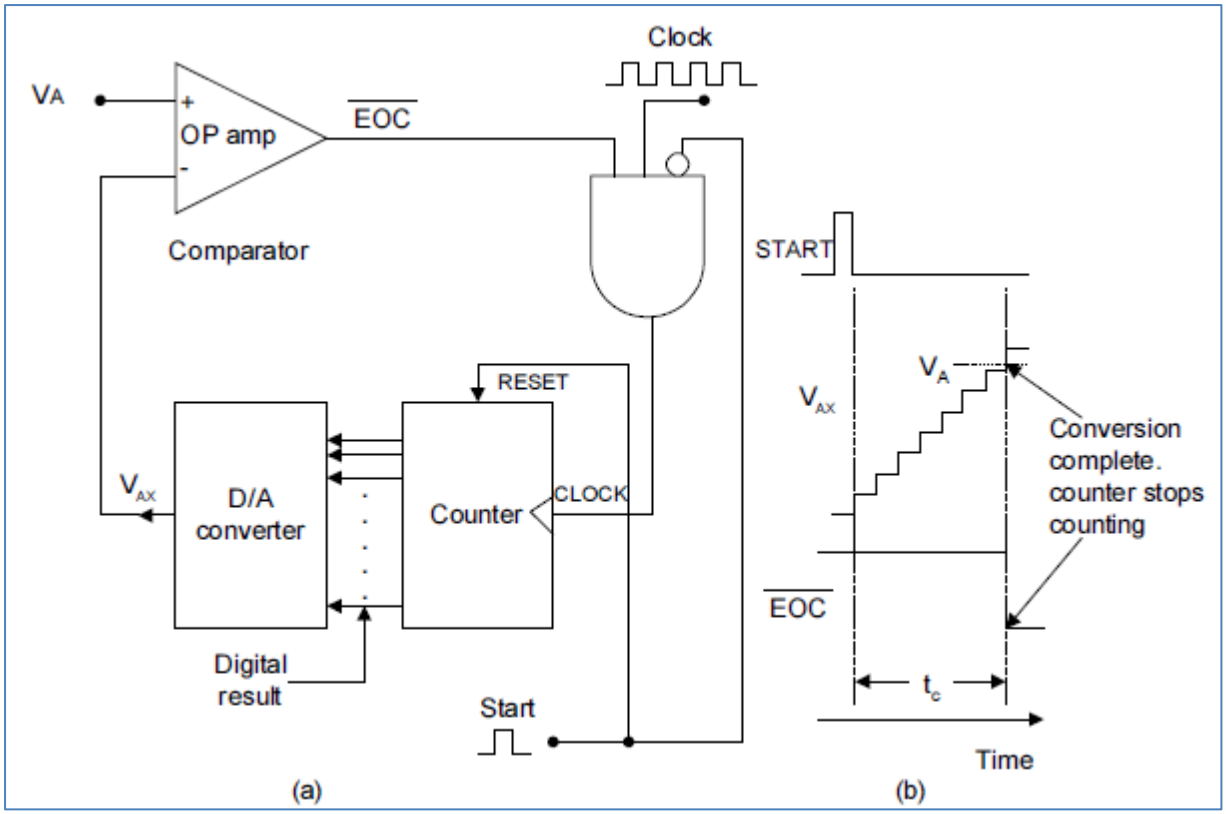
a) A three-bit Analogue to Digital Converter (ADC) is specified with a full-scale input voltage of 8 volts. Sketch the ideal transfer characteristic of this ADC. (5 marks)

b) Compare the conversion times of the successive approximation ADC and the integrating ADC. (2 marks)

c) A certain 8-bit DAC has a full-scale output of 2mA and a full-scale error of ± 0.5% Full Scale. What is the range of possible outputs for an input of 10000000? (3 marks)

d) Define/Describe settling time and offset error as applicable to DACs performance (2 marks)

e) The 8-bit ADC below has a full-scale input of 2.55 V (i.e., V_A = 2.55 V produces a digital output of 11111111). It has a specified error of 0.1% Full Scale. Determine the maximum amount by which the V_{AX} output can differ from the analog input. (3 marks)



f) The performance of the DAC can be described in a number of ways, including:

- the number of input bits;
- the voltage range for the output;
- the step size for the output voltage;
- the speed of conversion;
- the power supply used.

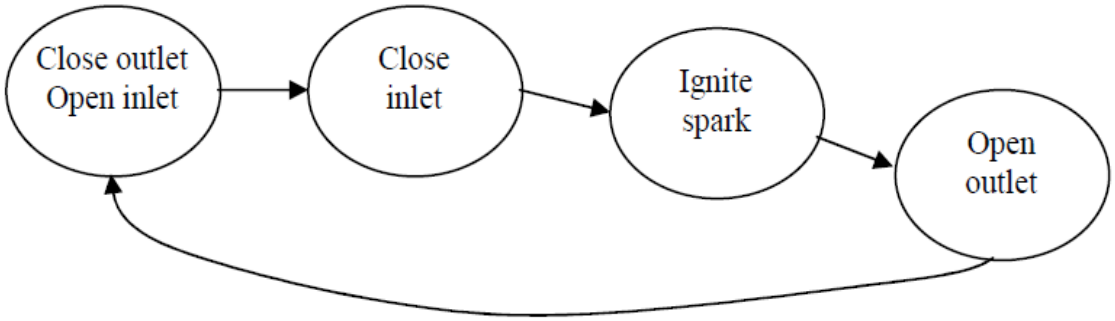
Design a DAC with the following parameters:

- number of input bits = 4;
- output voltage range = 0 to 12V;
- logic 1 = 8V and logic 0 = 0V;
- power supply = +15V / 0V / -15V. (5 marks)

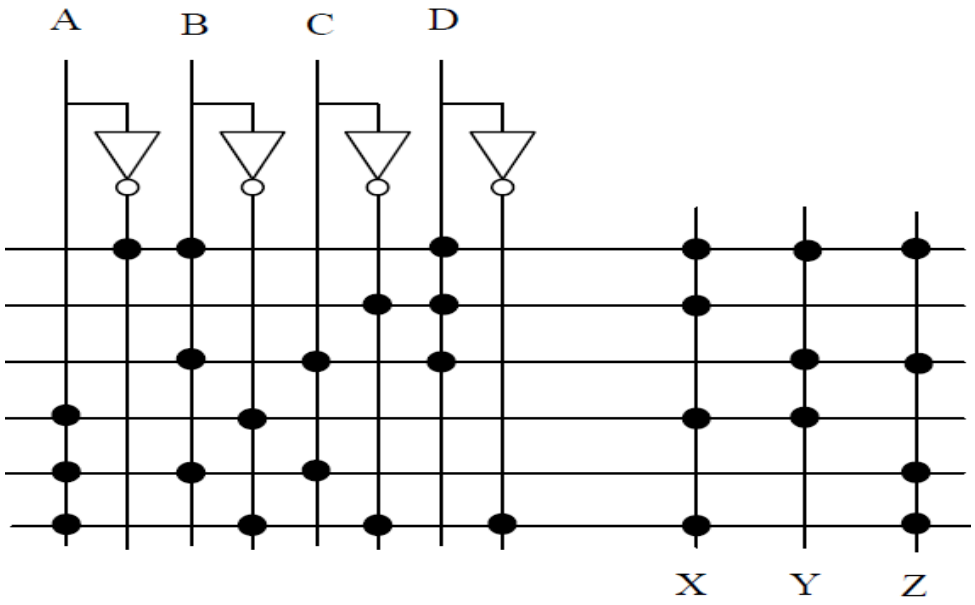
QUESTION FIVE (20 MARKS)

a) An engine needs to go through four strokes, all of equal duration (see figure below for state sequence). On the first stroke the inlet valve is open and the outlet is closed; on the second stroke the inlet is closed; on the third stroke a spark is delivered; and the forth stroke the outlet is open for the exhaust from the explosion to vent. Then the first stroke comes again and the cycle repeats. Design a controller for the system, with a clock for input and with

three outputs: one to open the inlet, one to open the outlet, and one to ignite the spark. Assume that if the control to open a valve isn't asserted, the valve closes (spring-loaded valve). The frequency of the clock will determine the speed of engine. Use JK Flip flops in your design. (10 marks)



b) The internal connection diagram for a PLA is given below.



i. Write the equations realized by the PLA. (5 marks)

ii. Specify the truth table for a ROM which would realize the same function. (5 marks)