MACHAKOS UNIVERSITY

University Examinations for 2018/2019

SCHOOL OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF COMPUTING AND INFORMATION TECHNOLOGY

THIRD YEAR SPECIAL/SUPPLEMENTARY EXAMINATION FOR

BACHELOR OF SCIENCE (INFORMATION TECHNOLOGY)

SIT311: COMPUTER ARCHITECTURE

DATE: 26/7/2019 **TIME: 2.00-4.00 PM**

INSTRUCTIONS

Answer **question ONE and any other TWO questions.**

QUESTION ONE

a) Explain the functions of the following components of von Neumann computer architecture (4 marks)

i. Arithmetic and Logic Unit (ALU)

ii. System RAM

b) Write the **TWO's** and **ONE's** Complement of -53_{10} (4 marks)

c) Convert -210.25_{10} into IEEE 754 binary floating point single precision representation (4 marks)

d) With aid of diagrams explain the difference between register and stack addressing modes (6 marks)

e) Explain the function of the following CPU registers (4 marks)

a. Program counter

b. Index register

d) Describe the difference between CISC and RISC architectures (6 marks)

e) Explain how Cache memory helps to speed up instruction execution by the CPU (2 marks)

QUESTION TWO

a) With aid of diagrams explain the difference between Set Associative and Fully Set Associative cache mappings (6 marks)

b) State THREE elements of an instruction (3 marks)

c) Describe the computer memory hierarchy (8 marks)

d) State one advantage and two disadvantages of assembly programming languages (3 marks)

QUESTION THREE

a) State the Amdahl's Law (2 marks)

b) Floating point instructions are improved to run twice as fast, but only 10% of the time was spent on these instructions originally.

   a. How much faster is the new machine? (4 marks)

   b. How much faster would the new machine be if floating point instructions become 80 times faster? (4 marks)

c) Explain the difference between Hardwired and Micro-Programed Control Units (6 marks)

d) With aid of block diagrams explain the differences Von Neumann and Harvard Computer architectures (4 marks)

QUESTION FOUR

Assume that to spell check a large file, 820,000,000 instructions are needed. The instructions in the program are broken down into 4 different classes, and each class requires N clock cycles to execute. Specific information is given in the table below.

Instruction class	**t**	**Number of instructions**
Branch	3	150,000,000
Store	4	185,000,000
Load	5	260,000,000
ALU	4	225,000,000

Question A: (10 marks)

If the total execution time for this program is found to be 1.57 seconds, what is the clock cycle time of the computer in nanoseconds on which it was run?

Question B: (10 marks)

Assume that as part of the 820,000,000 instruction spell check, 25% of all load instructions are immediately followed by an ALU / R-type instruction that uses the data that was just loaded. To speed up this program, we are contemplating adding a new type of instruction – an ALU instruction where one of the source operands is a value from memory.

- This new instruction will replace the previous, 2 instruction sequence.

- It will take 7 clock cycles.

Will this change offer any speedup over the original design? If so, how much?

NB: Assume that the clock rate does not change

QUESTION FIVE

a) Briefly explain CPU instruction execution cycle (6 marks)

b) Convert 2.25 into IEEE 754 binary floating point double precision representation (5 marks)

c) Explain three ways in which CPU execution time can be decreased (6 marks)

d) Explain the difference between dynamic and Static RAM (3 marks)