MACHAKOS UNIVERSITY

University Examinations for 2021/2022

SCHOOL OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

THIRD YEAR SECOND SEMESTER EXAMINATIONS FOR BACHELOR OF SCIENCE IN ELECTRICAL AND ELECTRONICS ENGINEERING

EEE 306: DIGITAL ELECTRONICS II

DATE: 15/12/2021 **TIME: 8.30-10.30 AM**

INSTRUCTIONS

ANSWER QUESTION ONE AND ANY OTHER TWO

QUESTION ONE (30 MARKS)

(a) For a 4×1 Multiplexer, give the truth table and the gate-level circuit implementation of the same. (5 marks)

(b) Show how the full adder can be implemented using a decoder of your choice and OR gates. (6 marks)

(c) Differentiate between combinational and sequential logic circuits. (4 marks)

(d) Show the implementation of the following Boolean function using a 8×1 multiplexer. (5 marks)

$$F = \Sigma\,(0, 2, 5, 7, 11, 14)$$

(e) Differentiate between a PLA, PAL and PROM in terms of the AND and OR arrays.

(3 marks)

(f) Design a 3-bit counter which counts in the sequence: 001, 011, 010, 110, 111, 101, 001.

Use clocked T flip-flops. (7 marks)

QUESTION TWO (20 MARKS)

(a) Implement the logic function below using a 4×1 Multiplexer. (6 marks)

$$F(x, y, z) = \Sigma(1, 2, 6, 7)$$

(b) Design a combinational circuit using a ROM. The circuit accepts a 3-bit number and generates an output binary number equal to the square of the input number. (6 marks)

(c) A 6-bit R-2R ladder D/A converter has a reference voltage of 6.5V. It meets standard linearity.

Find: (i) The Resolution in Percent.

(ii) The output voltage for the word 011100. (4 marks)

(d) 6-bit Dual Slope A/D converter uses a reference of –6V and a 1 MHz clock. It uses a fixed count of 40 (101000). Find Maximum Conversion Time. (4 marks)

QUESTION THREE (20 MARKS)

(a) Show how the functions below can be implemented using a PLA. (6 marks)

$F1 = AB'+AC+A'BC'$

$F2 = (AC+BC)'$

(b) With the help of a neat diagram, explain the working of a successive approximation A/D converter. (6 marks)

(c) Implement a 1×8 demultiplexer using 1×4 demultiplexers. (4 marks)

(d) Implement a 3 to 8 decoder using 2 to 4 decoders. (4 marks)

QUESTION FOUR (20 MARKS)

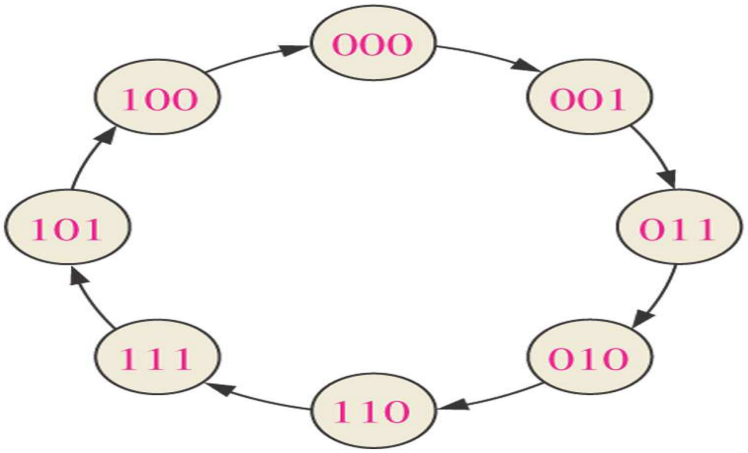
(a) Implement the full adder circuit using a dual 4×1 multiplexer. (6 marks)

(b) Implement the functions below using a decoder and OR gates. (4 marks)

$$F_1 = x(y + y')z = x'y'z' = \Sigma(0, 5, 7)$$
$$F_2 = xy'z' + x'y + x'y(z + z') = \Sigma(2, 3, 4)$$
$$F_3 = x'y'z + xy(z + z') = \Sigma(1, 6, 7)$$

(c) A certain 8-bit DAC has a full-scale output of 2mA and a full-scale error of ± 0.5% Full Scale. What is the range of possible outputs for an input of 10000000? (3 marks)

(d) Design a three bit gray counter whose state diagram is shown below using JK flip flops. (7 marks)



QUESTION FIVE (20 MARKS)

We wish to design a sequence detector circuit, which detects three or more consecutive 1's in a string of bits coming through an input line.

(a) Find the state diagram. (4 marks)

(b) Determine the type of the circuit (Moore or Mealy model). (3 marks)

(c) Tabulate state (or transition) table of sequence detector. (5 marks)

(d) Implement the circuit using D and J-K flip-flops. (8 marks)