MACHAKOS UNIVERSITY

University Examinations for 2024/2025 Academic Year

SCHOOL OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

THIRD YEAR FIRST SEMESTER EXAMINATION FOR DEGREE IN BACHELOR OF SCIENCE IN TELECOMMUNICATION

SPH 312: COMPUTER ARCHITECTURE AND ORGANIZATION

DATE: 14TH JANUARY 2025 **TIME: 11.00 AM - 1.00 PM**

INSTRUCTIONS:
*Answer question **ONE (Compulsory)** and **any other TWO** questions*

QUESTION ONE *(COMPULSORY)* (30 MARKS)

(a) Draw a block diagram showing the main sections of a microcomputer and illustrate the information flow between them. (4 marks)

(b) Explain the difference between multiplexed and non multiplexed bus systems. (2marks)

(c) Describe three characteristics of CPLDs and FPGAs (6marks)

(d) Design a circuit to take a 4bit number ABCD and produce a single output Y that is true only if the inputs represents a prime number. (10marks)

(e) Explain the difference betwen PLAs, PALs and PROMs (6marks)

(f) Explain the meaning of the term byte sexing. (2marks)

QUESTION TWO (20 MARKS)

(a) Draw and lable a diagram of a typical microcomputer bus system. (6marks)

(b) Using a karnaugh map,simplify the following function.

F=ABC'D+A'BCD+AB'C'D+A'BCD+A'B'C'D+ABC'D' (6marks)

(c) Generate a logic diagram from a boolean expression below

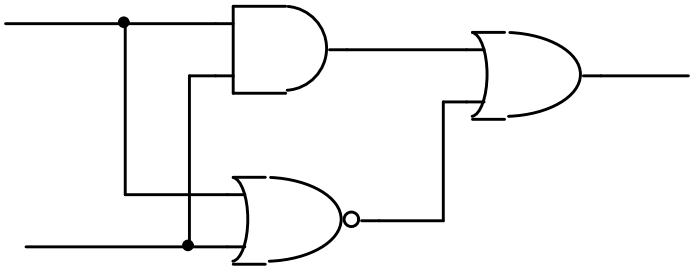
C=AB+A''B''+(A+B) (8marks)

QUESTION THREE (20 MARKS)

(a) Give three diferences between ROM and RAM (6marks)

(b) With an aid of a well labled diagram, illustrate the computer configuration. (10 marks)

(c) Extract the boolean expression from the below diagram



QUESTION FOUR (20 MARKS)

(a) List the main components of a CPU describing the functioning of each. (6marks)

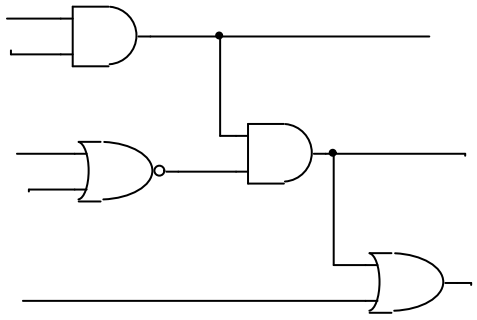
(b) Calculate the number of address lines required for the following memory devices

(i) A 64 kbyteROM

(ii) A 2kbyte RAM

(iii)A 64kbit (8k X 8bit)ROM (6marks)

(c) Derive boolean expressions to desribe the operation of the following circuit. Minimize this expressions by algebraic manipulation. (8marks)



QUESTION FIVE (20 MARKS)

a) Design a BCD to seven segment decoder which takes a 4 bit input reresenting a number in the range of 0-9 and generate an appropriate 7bit output to illuminate the appropriate elements. (10marks)

b) A digital system is to be designed with two inputs and three outputs. The system should function under the following conditions

i) Out put ***x*** indicates the absence of both inputs

ii) Output ***y*** indicates the presence of either input and absence of the other.

iii) Output ***z*** indicates the presence of both inputs

Using logic equitions and truth table:

a) Draw the logic diagram for the systemusing the minimum number of gates.

b) Modify your logic diagram to its simplest form using NAND gates only

(10marks)