MACHAKOS UNIVERSITY

University Examinations for 2020/2021 Academic Year

SCHOOL OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

SECOND YEAR SECOND TERM EXAMINATION FOR

DIPLOMA IN ELECTRICAL AND ELECTRONICS ENGINEERING

2601/202D: DIGITAL ELECTRONICS

DATE: 3/6/2021 **TIME: 8.30-11.30 AM**

INSTRUCTIONS

1. You should have an examination booklet for this examination
2. This paper has **FIVE** questions.
3. Answer **ALL** questions.
4. Maximum marks for each part of a question are as shown.

QUESTION ONE (20 Marks)

a) i State Demorgans Theorem. (2 marks)

ii Define the following terms;

I. Flip Flop

II. Counter

III. Register (6 marks)

iii State TWO applications of decoders (2 marks)

b) With the aid of waveforms, design a Mod. 10 UP- ripple counter. (10 marks)

QUESTION TWO (20 MARKS)

a) An alarm system is needed to maintain three boilers in an industrial plant. Three sensors monitor water level (A), Temperature (B) and pressure (C). The system provide a high signal that can be connected to a buzzer, if the water level is low and the temperature is too high, or if the water level is low and the pressure is too high, or if the water level is low and

the temperature and the pressure is too high, if the water level is high and the temperature or pressure is too high.

i. Draw a truth table to represent the system conditions.

ii. Write down the Boolean expression for the alarm system and simplify it using a K-Map.

iii. Design a logic circuit to implement the system. (10 marks)

b) With the aid of waveforms, design a Modulo 12 UP- ripple counter. (10 marks)

QUESTION THREE (20 MARKS)

a) i Draw the symbol of a S-R flip-flop. (2 marks)

ii With the aid of a logic diagram and truth table, describe the operation of a clocked D flip-flop. (10 marks)

b) With the aid of a block diagram, truth table and logic circuit diagram, design a 3 to 8 line Decoder. (8 marks)

QUESTION FOUR (20 MARKS)

a) State the operational differences between synchronous and asynchronous counters. (2 marks)

b) A 4-bit counter has a propagation delay time (t_{pd}) of 50nS for each flip flop and a propagation delay time (t_{pd}) of 20nS for each AND gate used.

i. Determine the maximum frequency (f_{max}) when the counter is connected as;

- Synchronous counter
- Ripple counter. (6 marks)

ii Compare the results in (b) (i) above. (2 marks)

c) i Draw the logic circuit diagram of a 5-bit twisted ring counter

ii Determine the auxiliary states of (c) (i) above. (10 marks)

QUESTION FIVE (20 MARKS)

a) With the aid of a logic circuit diagram describe the operation of a four-bit Parallel-in Serial-out Shift Register using D-type flip-flops. (10 marks)

b) Implement the following expression using a Multiplexer

$F(A, B, C) = \sum_m (0, 2, 4, 6)$. (10 marks)