MACHAKOS UNIVERSITY

University Examinations for 2018/2019

SCHOOL OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF COMPUTING AND INFORMATION TECHNOLOGY

SECOND YEAR SECOND SEMESTER EXAMINATION FOR

BACHELOR OF SCIENCE (COMPUTER SCIENCE)

SCO 201: COMPUTER ORGANIZATION AND ARCHITECTURE II

DATE: 30/4/2019 **TIME: 2.00-4.00 PM**

INSTRUCTIONS

Answer **question ONE and any other TWO questions.**

QUESTION ONE (COMPULSORY)

a) Describe the kinds of addressing modes below with an example (9 marks)

i. Immediate addressing mode

ii. Register indirect addressing mode

iii. Displacement addressing mode

b) Explain any two input output modes of data transfer. (6 marks)

c) Define an instruction and with example explain three, one, zero address instructions. (8 marks)

d) Identify the problem with the following register transfer statements (3 marks)

(i) $xT : AR \leftarrow AR,\ AR \leftarrow 0$

(ii) $yT : R_1 \leftarrow R_2,\ R_1 \leftarrow 0$

(iii) $zT : PC \leftarrow AR,\ PC \leftarrow PC + 1$

e) Using memory organization, answer the questions below (4 marks)

i. A computer has 32MB (megabytes) of memory. How many bits are needed to address any single byte in memory?

ii. A computer has 128MB of memory. Each word in this computer is eight bytes. How many bits are needed to address any single word in memory?

QUESTION TWO (20 MARKS)

a) Suppose you are designing a computer from scratch and that your company's budget allows a very small amount of memory bandwidth. Explain briefly some of the characteristics you will choose in the ISA and the microarchitecture. (8 marks)

b) Explain three types of Instruction with examples (6 marks)

c) Using a RAM organization diagram, Explain a 7 bit data and 4 bit address memory. (6 marks)

QUESTION THREE (20 MARKS)

a) Explain in detail about interrupt handling in computers (8 marks)

b) Explain the working of a Microprogram Sequencer with the help of a neat diagram. (7 marks)

c) Explain the different mapping techniques used for cache memory (5 marks)

QUESTION FOUR (20 MARKS)

a) Define instruction pipeline and explain two reasons that often prevent the pipeline from staying full with useful instructions (in two words each) (4 marks)

b) Draw a diagram of three bus structure of processor organization and describe Bus Arbitration (10 marks)

c) Draw the instruction state cycle diagram (6 marks)

QUESTION FIVE (20 MARKS)

a) We have a byte-addressable toy computer that has a physical address space of 512 bytes. The computer uses a simple, one-level virtual memory system. The page table is always in physical memory. The page size is specified as 8 bytes and the virtual address space is 2 KB. Suppose that we would like to add a 128-byte *write-through* cache to enhance the performance of this computer. However, we would like the cache access and address translation to be performed simultaneously. In other words, we would like to index our cache using a virtual address, but do the tag comparison using the physical addresses (virtually-indexed physically-tagged). The cache we would like to add is direct-mapped, and has a block size of 2 bytes. The replacement policy is LRU. Answer the following questions:

   i. How many bits of a virtual address are used to determine which byte in a block is accessed? (2 marks)

   ii. How many bits of a virtual address are used to index into the cache? Which bits exactly (2 marks)

   i. What is the size of the tag store in bits? Show your work. (4 marks)

b) Compare the characteristics of CISC and RISC (6 marks)

c) Differentiate between hardwired control and micro programmed control (6 marks)