MACHAKOS UNIVERSITY

University Examinations 2016/2017

SCHOOL OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

THIRD SEMESTER EXAMINATION FOR BACHELOR OF SCIENCE IN ELECTRICAL AND ELECTRONICS ENGINEERING

SUPPLEMENTARY EXAMINATIONS

EEE 308: ANALOGUE ELECTRONICS I

DATE: **TIME: 2 HRS**

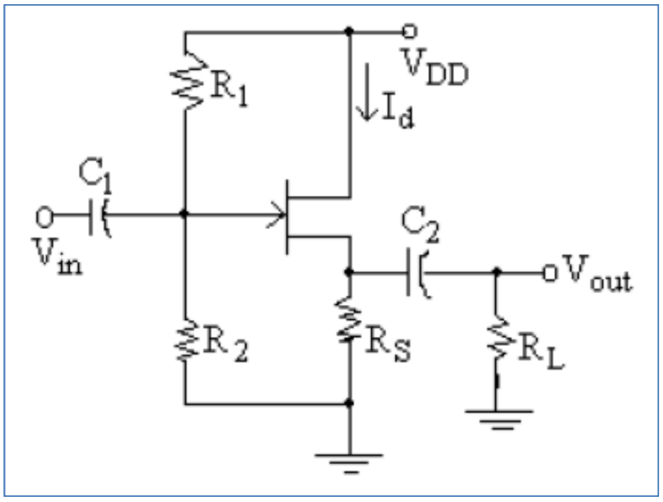
INSTRUCTIONS.

Answer **QUESTION ONE** and **any other TWO.**

Do **NOT** answer **MORE** than **three** questions.

QUESTION ONE (30 MARKS)

(a) The FET circuit given below in Fig.1, has R_1=3.5MΩ, R_2 = 1.5MΩ, R_S = 2KΩ, R_L = 20KΩ and g_m = 2.5mS. Find its input impedance, output impedance and voltage gain. (8mks)



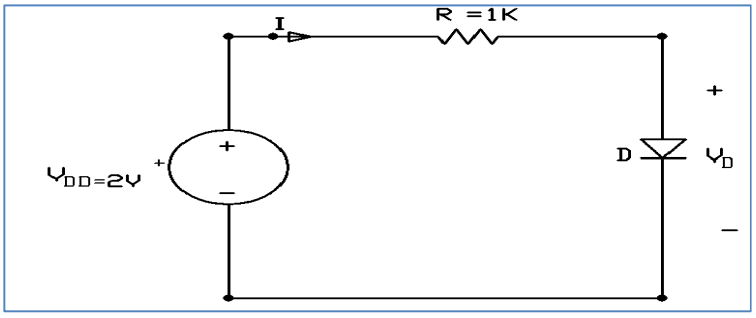
(b) A half-wave rectifier has a load resistance of 3.5 KΩ. If the diode and secondary of the transformer have a total resistance of 800KΩ and the ac input voltage has 240 V (peak value), determine:
(i) peak, rms and average values of current through load
(ii) DC power output
(iii) AC power input
(iv) rectification efficiency (7 marks)

(c) A BJT has a base current of 250 μA and emitter current of 15mA. Determine the collector current gain and β. (5 marks)

(d) Explain the physical operation of diodes using a suitable current-voltage characteristic sketch. (5 marks)

(e) Determine the current I in the circuit below using the CVD model and assuming a silicon diode. What will be the consequence of having $V_{DD} = 0.5\,V$. Explain your answers clearly.

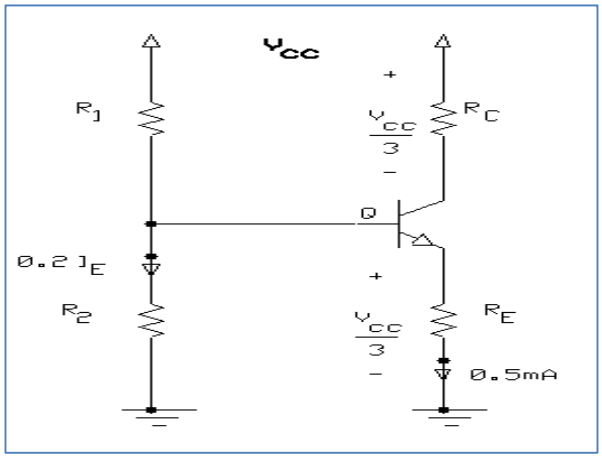
(5 marks)



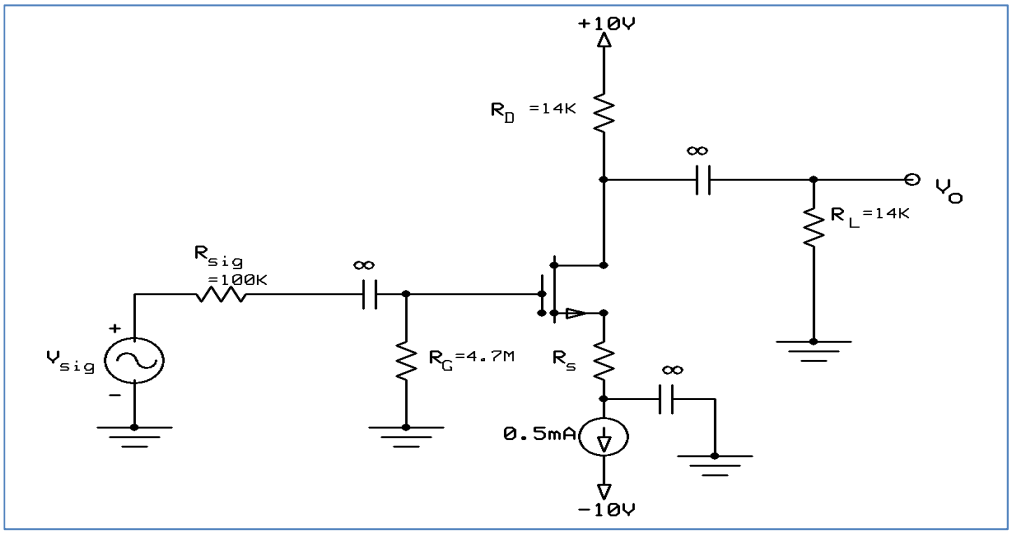
QUESTION TWO (20 MARKS)

(a) A full wave rectifier is fed with a voltage, 50 sin 100πt. Its load resistance is 400Ω. The diodes used in the rectifier have an average forward resistance of 30Ω. Compute the
(i) average and rms values of load current,
(ii) ripple factor and
(iii) efficiency of rectification. (8 marks)

(b) Design the bias circuit below for a V_{CC}=9 V to provide 3 V across R_E and RC, I_E=0.5 mA, and the voltage divider current of $0.2I_E$, as shown. (6 marks)

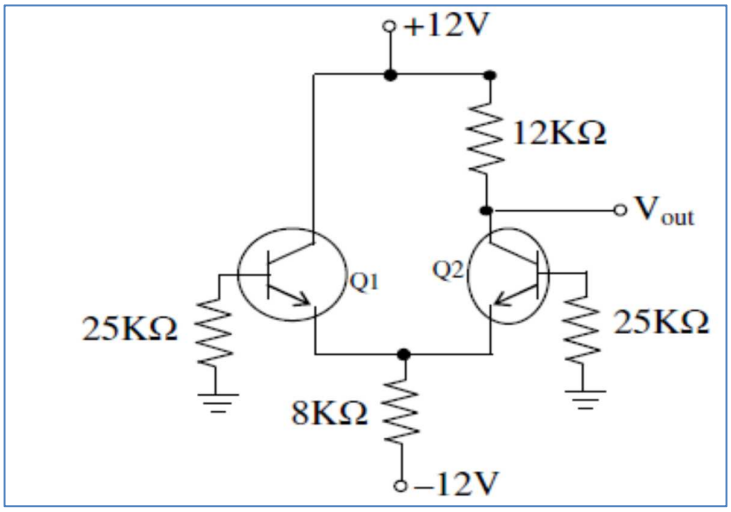


(c) Compute the small-signal voltage gain for the circuit below with $R_S = 0$, $k'_n W/L = 1\ mA/V^2$, and $V_t = 1.5\ V$. For a 0.4 V_{pp} sinusoidal input voltage, what is the amplitude of the signal? (6 marks)

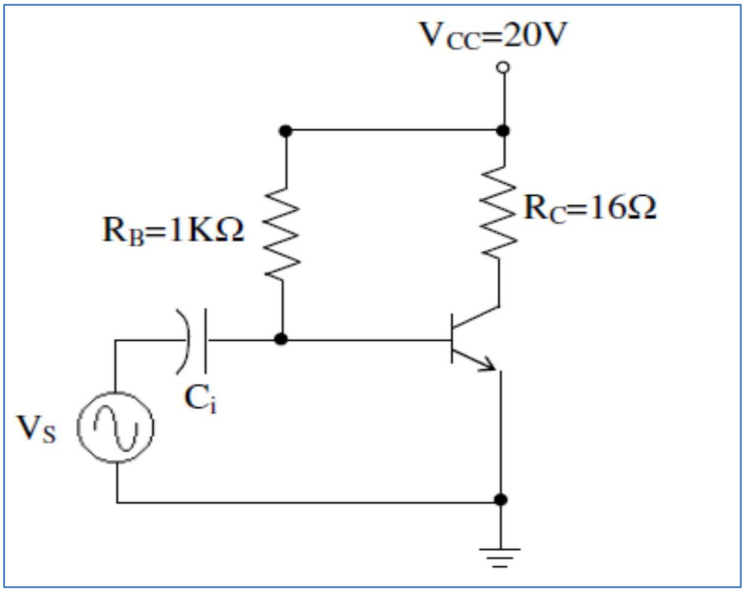


QUESTION THREE (20 MARKS)

(a) In the differential amplifier circuit shown below, the transistors have identical characteristics and their β=100.Determine the (i) output voltage (ii) base currents and (iii) base voltages taking into account the effect of the R_B and V_{BE}. Take V_{BE}=0.7 Volts. (10 marks)



(b) The power amplifier shown below is operated in class A, with a base current drive of 8.5mA peak. Calculate the input dc power, the power dissipated in the transistor, the signal power delivered to the load and the overall efficiency of the amplifier, if transistor β=30 and V_{BE}=0.7V. (10 marks)



QUESTION FOUR (20 MARKS)

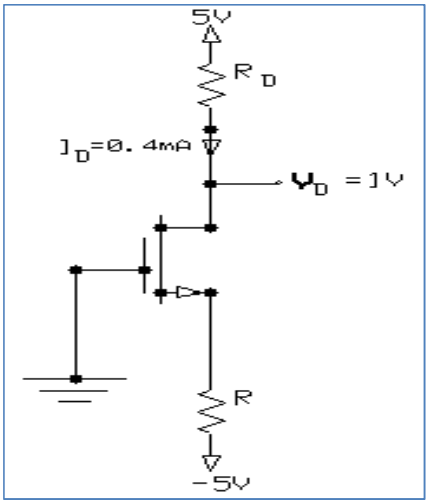
(a) In a transistor amplifier, a change of 0.025V in signal voltage causes the base current to change by 15μA and collector current by 1.2 mA. If collector and load resistances are of 6kΩ and 12kΩ, determine
(i) input resistance (ii) current gain iii) ac load (output resistance) (iv) voltage gain (v) power gain (10 marks)

(b) The transconductance of a FET used in an amplifier circuit is 4000 micro-siemens. The load resistance is 15kΩ and drain circuit resistance is 10 MΩ. Calculate the voltage gain of the amplifier circuit . (5 marks)

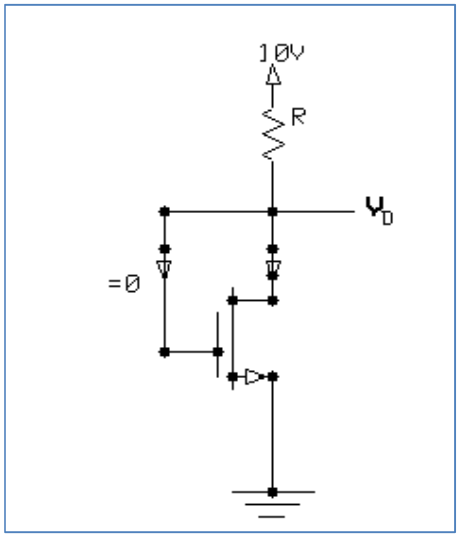
(c) State the differences between *pnp* and *npn* transistors. (5 marks)

QUESTION FIVE (20 MARKS)

(a) Design the circuit below so that the MOSFET operates with I_D= 0.4 mA and V_D=1 V. The MOSFET has V_t=2 V, $\mu_n C_{ox} = 20\ \mu A/V^2$, L=10 μm, with W=400 μm. Neglect the channel-length modulation effect ($\lambda = 0$). (5mks)



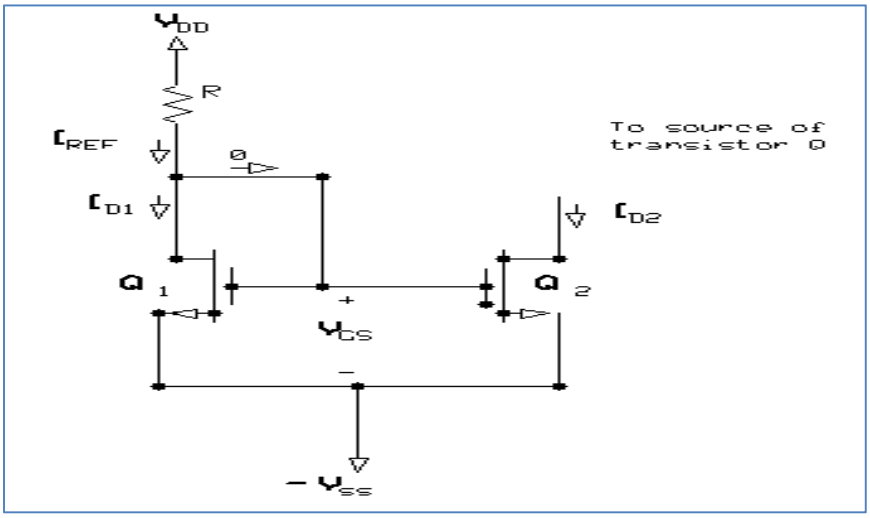
(b) Design the circuit below so I_D= 0.4 mA and V_D=1 V. The MOSFET has V_t=2 V, $\mu_n C_{ox} = 20\ \mu A/V^2$, L=10 μm, with W=100 μm. Neglect r_o. (5 marks)



(c) (i) Design an NMOS current mirror below with VDD=5 V, VSS=0, and I_{REF}=100 µA.

For the matched transistors L=10 μm, with W=100 μm, V_t=1 V, and $k_n' = 20\frac{\mu A}{\ }\ V^2$.

(5 marks)



(ii) For your design, what is the lowest possible value for $V_O=V_{D2}$ and still have a functioning current mirror? (2 marks)

(iii) Imagine that $V_A=10^7$ L. (Notice that V_A is proportional to the channel length, which is commonplace). What is r_o? (2 marks)

(iv) What is change in the output current I_O if V_O changes by 3 V? (1mark)