MACHAKOS UNIVERSITY

University Examination 2018/2019

SCHOOL OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

THIRD YEAR SECOND SEMESTER EXAMINATION FOR

BACHELOR OF SCIENCE (ELECTRICAL AND ELECTRONICS ENGINEERING)

EEE 306: DIGITAL ELECTRONICS II

DATE: 23/5/2019 **TIME: 8.30-10.30 AM**

INSTRUCTIONS

Answer Question ONE and any other TWO Questions.

QUESTION ONE (30 MARKS)

a) Implement the function below using 4×1 multiplexer. Apply *x* and *y* to the select lines.

$$F(x,y,z) = \Sigma m(1, 2, 6, 7)$$

(5 marks)

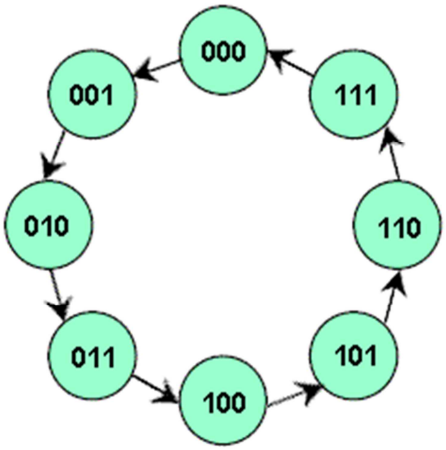
b) Draw the block diagram representation of a 8-Word×4-Bit ROM and give its truth table. (5 marks)

c) List down the three types of ROM devices and explain the differences between them. (6 marks)

d) Prepare the PLA programming table for the following functions. (4 marks)

$$F_0 = A'B' + AC'$$
$$F_1 = AC' + B$$
$$F_2 = A'B' + BC'$$
$$F_3 = B + AC$$

e) A counter is first described by a state diagram, which shows the sequence of states through which the counter advances when it is clocked. The figure below shows a state diagram of a 3-bit binary counter. Design the counter using JK flips flops. (10 marks)



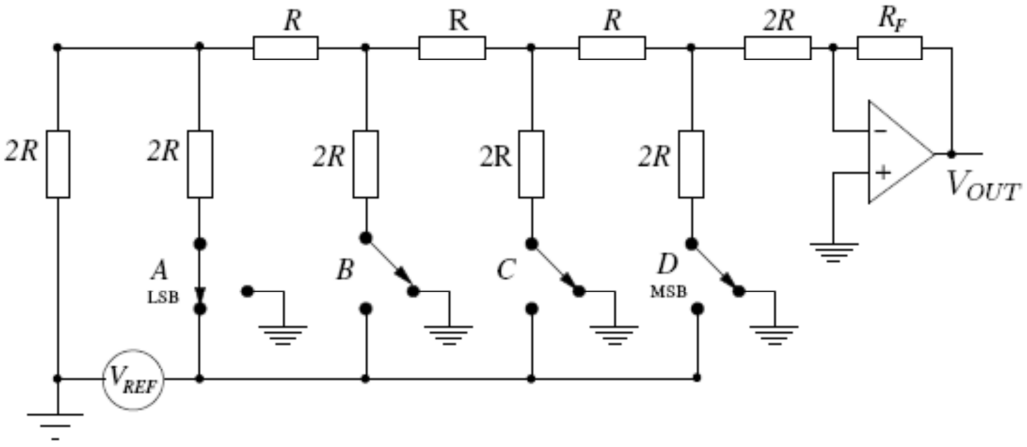
QUESTION TWO (20 MARKS)

a) Show the gate level implementation of a 1-to-4 demultiplexer. Draw the circuit diagram and explain how it works. (5 marks)

b) Draw the circuit diagram of a full adder and explain its working using a truth table. (5 marks)

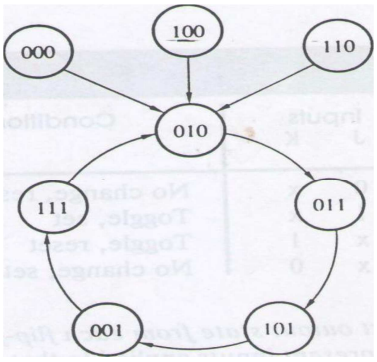
c) Design a 3-bit counter that advances through the sequence 000, 010, 011, 101, 110, 000 and repeats. Not all of the possible combinations of the 3 bits represent a valid state. The unused states, 001, 100, and 111, should be used as don't-care conditions to simplify the logic. Use T flip flops. (6 marks)

d) The R-2R ladder network uses resistors of only two sizes, R and 2R. Derive an expression for the output voltage of the R-2R ladder network shown below. (4 marks)



QUESTION THREE (20 MARKS)

a) Design a MOD-5, 3-bit synchronous counter to count in the following sequence: 2, 3, 5, 1, 7. The counter must be self-starting with the count states of 0, 4, and 6 leading directly to 2. The operation of the counter is shown in the state diagram below. Use JK flip flops. (6 marks)



b) Design a counter with the following counting sequence: 0, 1, 2, 4, 6 and repeat. Use D-flip flops. Do not use a decoder in your design. Treat the unused states as don't cares in your design. (6 marks)

c) Draw the internal logic of a 32×8 ROM. (4 marks)

d) Design a combinational circuit using a ROM. The circuit accepts a three bit number and outputs a binary number equal to the square of the input number. (4 marks)

QUESTION FOUR (20 MARKS)

a) Tabulate the PLA programming table for the four Boolean functions listed below. Minimize the product terms.(6 marks)

$$A(x, y, z) = \Sigma(1, 2, 4, 6)$$
$$B(x, y, z) = \Sigma(0, 1, 6, 7)$$
$$C(x, y, z) = \Sigma(2, 6)$$
$$D(x, y, z) = \Sigma(1, 2, 3, 5, 7)$$

b) Tabulate the truth table for a 8×4 ROM that implements the Boolean functions listed below. Considering now the ROM as a memory, specify the memory contents at addresses 1 and 4. (4 marks)

$$A(x, y, z) = \Sigma(0, 3, 4, 6)$$
$$B(x, y, z) = \Sigma(0, 1, 3, 7)$$
$$C(x, y, z) = \Sigma(1, 5)$$
$$D(x, y, z) = \Sigma(0, 1, 4, 5, 7)$$

c) The following is a table of a three-input, four-output combinational circuit. Tabulate the PAL programming table for the circuit and mark the fuse map in a PAL diagram. (6 marks)

Inputs			Outputs			
x	y	z	A	B	C	D
0	0	0	0	1	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	0	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1

d) What are the differences between static RAM and dynamic RAM? (4 marks)

QUESTION FIVE (20 MARKS)

a) A 6-bit Dual Slope A/D converter uses a reference of –6V and a 1 MHz clock. It uses a fixed count of 40 (101000). Find Maximum Conversion Time. (4 marks)

b) Determine the analog output voltage of 6-bit DAC (R-2R ladder network) with Vref as 5V when the digital input is 011100 (4 marks)

c) A 6-bit R-2R ladder D/A converter has a reference voltage of 6.5V. It meets standard linearity. Find

i. The Resolution in Percent.

ii. The output voltage for the word 011100. (4 marks)

d) Find the conversion time of a Successive Approximation A/D converter which uses a 2 MHz clock and a 5-bit binary ladder containing 8V reference. What is the Conversion Rate? (4 marks)

e) A microprocessor uses RAM chips of 1024 ×1 capacity.

i. How many chips will be required and how many address lines will be connected to provide capacity of 1024 bytes.

ii. How many chips will be required to obtain a memory of capacity of 16 K bytes? (4 marks)