MACHAKOS UNIVERSITY

University Examinations for 2019/2020 Academic Year

SCHOOL OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF COMPUTING AND INFORMATION TECHNOLOGY

SECOND YEAR SECOND SEMESTER EXAMINATION FOR

BACHELOR OF SCIENCE (COMPUTER SCIENCE)

SCO 201: COMPUTER ORGANIZATION AND ARCHITECTURE II

DATE: 24/11/2020 **TIME: 2.00-4.00 PM**

INSTRUCTIONS

Answer question ONE and any other TWO questions.

QUESTION ONE (30 MARKS) (COMPULSORY)

a) State three methods of data transfer from input/output devices (3 marks)

b) Given the instruction A+B=C, explain the sequence of operations involving RTN where appropriate (9 marks)

c) Explain the importance of the following registers (6 marks)

i. MAR

ii. Accumulator

iii. IBR

d) Draw a diagram of a functioning microprogrammed unit (6 marks)

e) Explain some key design decisions in instruction set characteristics (6 marks)

QUESTION TWO (20 MARKS)

a) A computer has128MB of memory. Each word in this computer is eight bytes.

i. Find the number of bits are needed to address any single word in memory (4 marks)

ii. Draw its bus structure (6 marks)

iii. Using block diagram, explain its memory organization (4 marks)

b) Describe to design a computer to address the challenges below (6 marks)

i. Time and space locality

ii. Limited main memory capacity

QUESTION THREE (20 MARKS)

a) Differentiate between register addressing mode and direct addressing mode by use of diagrams (3 marks)

b) Write an assembly language programme that multiplies 3 with 2, and displays the result (5 marks)

c) Describe the following conditional flags (6 marks)

i. N

ii. Z

iii. C

d) Using a well labelled diagram, differentiate between parallel and pipelined ALUs (6 marks)

QUESTION FOUR (20 MARKS)

a) A student in Machakos university opted for CISC over RISC architecture. Explain three reasons to support his decision (6 marks)

b) Explain the problems with is with the following register transfer statements (6 marks)

(i) $xT : AR \leftarrow AR, AR \leftarrow 0$

(ii) $yT : R_1 \leftarrow R_2, R_1 \leftarrow 0$

(iii) $zT : PC \leftarrow AR, PC \leftarrow PC + 1$

c) Using three and two address machines (5 marks)

d) Explain the application of logic microoperatioms (3 marks)

QUESTION FIVE (20 MARKS)

a) Discuss branch prediction using a branch prediction state diagram (6 marks)

b) Discuss the three sections of assembly language (6 marks)

c) We have a byte-addressable toy computer that has a physical address space of 512 bytes. The computer uses a simple, one-level virtual memory system. The page table is always in physical memory. The page size is specified as 8 bytes and the virtual address space is 2 KB. Suppose that we would like to add a 128-byte *write-through* cache to enhance the performance of this computer. However, we would like the cache access and address translation to be performed simultaneously. In other words, we would like to index our cache using a virtual address, but do the tag comparison using the physical addresses (virtually-indexed physically-tagged). The cache we would like to add is direct-mapped, and has a block size of 2 bytes. The replacement policy is LRU. Answer the following questions:

i. How many bits of a virtual address are used to determine which byte in a block is accessed? (2 marks)

ii. How many bits of a virtual address are used to index into the cache? Which bits exactly (2 marks)

iii. What is the size of the tag store in bits? Show your work. (4 marks)