MACHAKOS UNIVERSITY

University Examinations for 2023/2024 Academic Year

SCHOOL OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

FOURTH YEAR FIRST SEMESTER EXAMINATION FOR

BACHELOR OF SCIENCE (ELECTRICAL AND ELECTRONICS ENGINEERING)

EEE 403: ANALOGUE ELECTRONICS III

DATE: **TIME:**

INSTRUCTIONS

Instructions: Attempt question ONE (Compulsory) and any other TWO questions.

QUESTION ONE (COMPULSORY) (30 MARKS)

a) State any THREE important features of instrumentation amplifier. (3 marks)

b) Explain why op-amps are used most commonly as integrator and not as differentiator. (3 marks)

c) With the aid of a suitable diagram explain how external offset compensation network for an inverting amplifier. (5 marks)

d) Determine the output voltage of the following op-amp circuit shown in Figure Q1 (d).

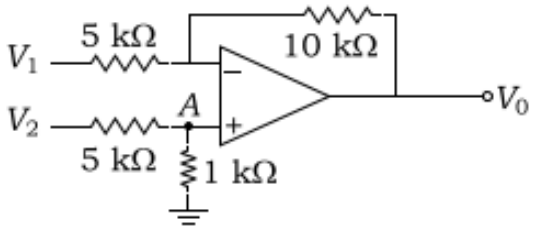

Figure Q1 (d)

(4 marks)

e) Using suitable diagrams discuss a comparator used as a zero crossing detector. (7 marks)

f) Prove that maximum collector efficiency of a Class B amplifier is 78.5%. (8 marks)

QUESTION TWO (20 MARKS)

a) Briefly explain the necessity of differential amplifier stage in construction of operational amplifiers. (3 marks)

b) Design and hence describe the working principle of first stage of an op-amp using bipolar junction transistors (BJT) and other relevant circuit components. (9 marks)

c) Operational amplifier has differential gain of 80 dB and CMRR of 100 dB. If $V_1 = 2\mu V$ and $V_2 = 1.6\mu V$, then calculate output voltages for differential and common-mode input signal operations. (8 marks)

QUESTION THREE (20 MARKS)

a) Explain the meaning of the term conversion efficiency as used in power amplifiers. (2 marks)

b) Discuss crossover distortion in power amplifiers and how it is minimized. (6 marks)

c) Draw the circuit diagram of a Class A amplifier and explain its operation briefly. (6 marks)

d) A Class A power amplifier has zero signal collector current of 50 mA. If the collector supply voltage is 5 V, determine:

i. The maximum ac power output,
ii. Power rating of the transistor, and
iii. Maximum collector efficiency. (6 marks)

QUESTION FOUR (20 MARKS)

a) Explain the following parameters of operational amplifier:

i. Slew rate
ii. CMRR (4 marks)

b) Show that the closed loop gain of practical inverting amplifier (assume finite open loop gain of A_{OL}) is given by

$$A_{CL} = \frac{-R_2/R_1}{1 + \frac{1}{A_{OL}}(1 + \frac{R_2}{R_1})}$$

(6 marks)

c) Determine the common-mode rejection ratio (CMRR) of the differential amplifier as shown in Figure Q4 (c).

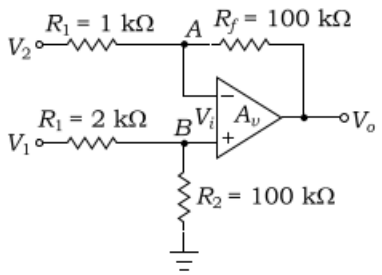

Figure Q4 (c)

(10 marks)

QUESTION FIVE (20 MARKS)

a) State THREE disadvantages of logarithmic amplifier. (3 marks)

b) Prove that the operational amplifier circuit as shown in Figure Q5 (b) is an integrator. Assume the operational amplifier is an ideal one. (6 marks)

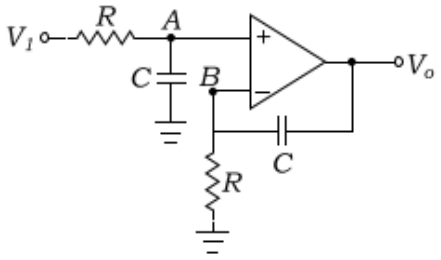

Figure Q5 (b)

c) Draw circuit diagram of a current to voltage converter and hence explain its operation. Give also a brief account of practical applications. (6 marks)

d) Explain the main problem with basic half-wave precision rectifier why it's rarely being used and hence illustrate how to remedy this problem. (5 marks)