MACHAKOS UNIVERSITY

University Examinations for 2022/2023

SCHOOL OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF COMPUTING AND INFORMATION TECHNOLOGY

THIRD YEAR SUPPLEMENTARY EXAMINATION FOR

BACHELOR OF SCIENCE (INFORMATION TECHNOLOGY)

SIT 311: COMPUTER ARCHITECTURE

DATE: 10/3/2023 **TIME: 2.00-4.00 PM**

INSTRUCTIONS: Answer Question ONE and other TWO Questions

QUESTION ONE (COMPULSORY) (30 MARKS)

a) State Amdahl's Law (In words, not a formula.) (1 mark)

b) Explain the purpose of the reference bit (sometimes called "access" bit) in a PTE (Page Table Entry). (2 marks)

c) A program spends 75% of its time doing multiply instructions. The multiplier is sped up by 3x.

i) How much faster does the application run? (Report your answer as "the program is X times faster.") (2 marks)

ii) Calculate the limit on the maximum speed-up if the multiplier in question (i) was infinitely fast. (Report your answer as "the program would be X times faster.") (2 marks)

d) Suppose you are designing a computer from scratch and that your company's budget allows a very small amount of memory bandwidth. Discuss THREE characteristics that you would choose in the ISA and the microarchitecture. (3 marks)

e) We want to compare the computers R1 and R2, which differ that R1 has the machine instructions for the floating-point operations, while R2 has not (FP operations are implemented in the software using several non-FP instructions). Both computers have a clock frequency of 400 MHz. In both we perform the same program, which has the following mixture of commands:

Type the command	Dynamic Share of instructions in program (p_i)	Instruction duration (Number of clock periods CPI_i)	
		R1	R2
FP addition	16%	6	20
FP multiplication	10%	8	32
FP division	8%	10	66
Non - FP instructions	66%	3	3

i. Calculate the MIPS for the computers R1 and R2. (4 marks)

ii. Calculate the CPU program execution time on the computers R1 and R2, if there are 12000 instructions in the program. (4 marks)

iii. From the above, in your opinion, at what mixture of instructions in the program will both computers R1 and R2 be equally fast? (1 mark)

f) On a computer with a 32-bit memory address, and the length of the memory location of 1 byte is installed set-associative cache. Cache size is 16 KB, block (line) size is 16 Bytes, set associative cache is 4-way.

i. Evaluate the number of sets that are there in cache. (4 marks)

ii. Show the bits in the memory address, which determine the address of the set. (2 marks)

iii. Show into which set is mapped the content of the memory address 10FFCFF(HEX). (2 marks)

g) A computer with virtual memory has an access time to main memory 50 ns, the time to transfer a block from the virtual into main memory is 10 ms. The probability for the page-fault is 10-6. Calculate the average access time, if the page-table is in the main memory. (3 marks)

QUESTION TWO (20 MARKS)

a) The fundamental distinction between interrupts and exceptions is that interrupts are caused by external events and exceptions are caused by events internal to the running process. Explain why Interrupts are handled mostly when convenient and give an example. (4 marks)

b) Discuss TWO techniques that eliminate the need for hardware-based interlocking in a pipelined processor. (4 marks)

c) Assume:

- A processor has a direct mapped cache
- Data words are *8 bits* long (i.e. 1 byte)
- Data addresses are *to the word*
- A physical address is *20 bits* long

- The tag is *11 bits*

- Each block holds 16 *bytes* of data

Evaluate the number of blocks are in this cache. (4 marks)

d) Minicomputers in the eighties (eg. DEC PDP-11) had 18 address signals and of course, the 18-bit address bus. Answer the following questions:

i. Evaluate the address space of these computers. (2 marks)

ii. Indicate what may have been the largest possible memory of these computers in bytes if the memory location is 1 Byte. (2 marks)

iii. Determine how long the program counter (PC) of these computers is. (2 marks)

iv. Explain what should be changed in these computers if we would like to increase address space 8-times. (2 marks)

QUESTION THREE (20 MARKS)

a) A virtual-to-physical address translation takes ~100 clock cycles; explain TWO most likely reasons for this particular latency. (4 marks)

b) We want to speed up computer performance with an additional unit for calculating in floating point format. This unit is 20 times faster than the same operations without unit. Calculate the percentage of a total computer time that this unit must be active to achieve an overall increase in computer speed for 2.5 times. (6 marks)

c) Assume that you have

- 4 Gbytes of main memory at your disposal

- 1 Gbyte of the 4 Gbytes has been reserved for process page table storage

- Each page table entry consists of:

  - A physical frame number
  - 1 valid bit
  - 1 dirty bit
  - 1 LRU status bit

- Virtual addresses are 32 bits

- Physical addresses are 26 bits

- The page size is 8 Kbytes

Determine the number of process page tables that can fit in the 1 Gbyte space. (6 marks)

d) Assuming that N instructions are executed, and all N instructions are add instructions, determine the speedup of a pipelined implementation when compared to a multi-cycle implementation. Your answer should be an expression that is a function of N. (4 marks)

QUESTION FOUR (20 MARKS)

a) Pipelining increases the performance of a processor if the pipeline can be kept full with useful instructions. Elaborate on TWO reasons that often prevent the pipeline from staying full with useful instructions. (4 marks)

b) The computer has a main memory access time of 60 ns. We want to reduce this time to 20 ns by adding cache. Determine how fast the cache must be (access time) if we can expect a 90% probability of a hit. (6 marks)

c) Computer with virtual memory has the following features:

- length of the virtual address is 38 bits,
- the page size is 16 KB,
- length of the physical address is 32 bits.

i. Evaluate the number of bits which is the length of page descriptor, if in addition to the frame number (FN), additional parameters occupy another 6 bits. (6 marks)

ii. Calculate the maximum size of the page-table in bytes. (4 marks)

QUESTION FIVE (20MARKS)

a) In your opinion, discuss the TWO most significant impediments to obtaining speedup from N cores on a multi-core chip (irrespective of finding a good parallel algorithm). (4 marks)

b) A cache may be organized such that:

- In one case, there are more data elements per block and fewer blocks
- In another case, there are fewer elements per block but more blocks

However, in both cases – i.e. larger blocks but fewer of them OR shorter blocks, but more of them – the cache's total capacity (amount of data storage) remains the same.

Discuss the pros and cons of each organization above. Support your answer with a short example assuming that the cache is direct mapped. (6 marks)

c) In a computer with cache, we have the average number of clock periods per instruction equal to 4, if there are no misses in the cache.

i. Determine the real number of clock periods per instruction, if the probability of miss in the cache is 10%. For the replacement of the block (line) in the cache, we need 5 clock periods for read and 10 for write accesses. Assume that each instruction requires an average of 2 memory accesses and that 20% of all are write accesses. (6 marks)

ii. Indicate what the real CPI will be, if we increase the probability of hit to 95%. (4 marks)