MACHAKOS UNIVERSITY

University Examinations for 2016/2017

SCHOOL OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

THIRD YEAR SECOND SEMESTER EXAMINATIONS FOR BACHELOR OF SCIENCE IN ELECTRICAL AND ELECTRONICS ENGINEERING

EEE 306: DIGITAL ELECTRONICS II

DATE: 19/6/2017 **TIME: 8:30 – 10:30**

INSTRUCTIONS

Answer Question One and Any Other Two Questions

QUESTION ONE (COMPULSORY) (30 MARKS)

(a) How is it possible to make a modulo 2^N counter using N-flip flops? Name the two types of such counters. (3 marks)

(b) Differentiate between a PROM, PLA and PAL. (3 marks)

(c) A microprocessor uses RAM chips of 1024 ×1 capacity.

(i) How many chips will be required and how many address lines will be connected to provide capacity of 1024 bytes.

(ii) How many chips will be required to obtain a memory of capacity of 16 K bytes. (4 marks)

(d) Design a mod-12 Synchronous up counter using D flip flops. Treat the unused states as don't care conditions in your design. Do not use a decoder in your design. (8 marks)

(e) What are synchronous counters? Design a Mod-5 synchronous counter using J-K Flip-Flops. Treat the unused states as don't care conditions in your design. (8 marks)

(f) A combinational circuit is specified by the following Boolean functions:

$$F_1(A, B, C) = \Sigma(3, 5, 6)$$
$$F_2(A, B, C) = \Sigma(1, 4)$$
$$F_3(A, B, C) = \Sigma(2, 3, 5, 6, 7)$$

Implement the circuit using a decoder constructed using NAND gates connected to the decoder outputs. Use a block diagram for the decoder and minimize the number of inputs in the external gates. (4 marks)

QUESTION TWO (20 MARKS)

(a) Derive the ROM programming table for the combinational circuit that squares a 4-bit number. Minimize the number of product terms. (7 marks)

(b) Tabulate the table for an 8x4 ROM that implements the Boolean functions below. Considering now the ROM as memory, specify the memory contents at addresses 1 and 4. (5 marks)

$$A(x, y, z) = \Sigma(0, 3, 4, 6)$$
$$B(x, y, z) = \Sigma(0, 1, 3, 7)$$
$$C(x, y, z) = \Sigma(1, 5)$$
$$D(x, y, z) = \Sigma(0, 1, 4, 5, 7)$$

(c) Design a combinational circuit using a ROM. The circuit accepts a three-bit number and outputs a binary number equal to the square of the input number. (5 marks)

(d) Draw the PLA circuit that implements the following functions. (3 marks)

$$F_1 = A'B + AC' + A'BC'$$

$$F_2 = (AC + AB + BC)'$$

QUESTION THREE (20 MARKS)

(a) With the help of R-2R binary network, explain the working of a 3-bit D/A converter and derive an expression for the output voltage. (8 marks)

(b) What are the specifications/ characteristics used by the manufacturers to describe a digital to analog converter? Explain each one briefly. (4 marks)

(c) Find the conversion time of a Successive Approximation A/D converter which uses a 2 MHz clock and a 5-bit binary ladder containing 8V reference. What is the Conversion Rate? (4 marks)

(d) A 6-bit R-2R ladder D/A converter has a reference voltage of 6.5V. It meets standard linearity. Find

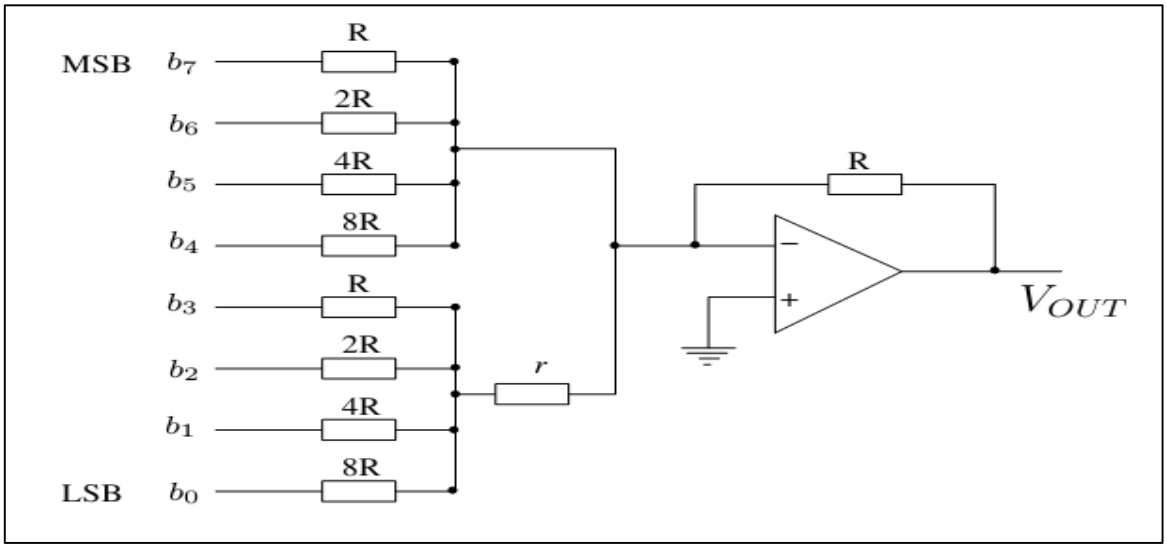
(i) The Resolution in Percent.

(ii) The output voltage for the word 011100. (4 marks)

QUESTION FOUR (20 MARKS)

(a) A 6-bit Dual Slope A/D converter uses a reference of –6V and a 1 MHz clock. It uses a fixed count of 40 (101000). Find Maximum Conversion Time. (4 marks)

(b) The weighted resistor DAC can be modified to accommodate a large number of bits without consequent spread in resistor values. An 8-bit modified weighted resistor DAC is shown in figure below. Obtain an expression for the resistor *r*. (6 marks)



(c) (i) A 2-bit flash converter has an input voltage range of 2.0V. What is its resolution?

(ii) What is the input voltage range of an 8-bit flash converter that has a resolution of 0.05V? (4 marks)

(d) Design a flash ADC with the following parameters:

- number of output bits = 2;
- input voltage range = 0 to 3V;
- comparator outputs have positive saturation = +12V and negative saturation = 0V;

Your design should include:

- a circuit diagram for the ADC with component values and reference voltage labelled;
- the resolution of the ADC;
- a table showing the operation of the circuit;
- Boolean expressions for the outputs of the priority encoder in terms of the inputs. (6 marks)

QUESTION FOUR (20 MARKS)

(a) Using a decoder and external gates, design the combinational circuit defined by the following three Boolean functions:

(i) $F_1=x'y'z'+xz$

$F_2=xy'z'+x'y$

$F_3=x'y'z+xy$

(ii) $F_1=(y'+x)z$

$F_2=y'z'+xy'+yz'$

$F_3=(x'+y)z$ (10 marks)

(b) Implement the following Boolean functions with a 8x1 multiplexer.

(i) $F(A, B, C, D)= \sum(0,2,5,7,11,14)$

(ii) $F(A, B, C, D)=\prod(3,8,12)$ (8 marks)

(c) Design a 32:1 multiplexer using two 16:1 multiplexers and a 2x1 multiplexer.

(2 marks)