



Machakos University College

(A Constituent College of Kenyatta University)

UNIVERSITY EXAMINATIONS 2013/2014

SCHOOL OF COMPUTING AND APPLIED SCIENCE

**SECOND YEAR SECOND SEMESTER EXAMINATION FOR THE DEGREE OF
BACHELOR OF SCIENCE (COMPUTER SCIENCE)**

SCO201: COMPUTER ORGANISATION AND ARCHITECTURE II

DATE: 9/4/2014

TIME: 8.30 a.m. – 10.30 a.m.

Answer question ONE and any other TWO questions in this paper

1.
 - a) Explain the following types of instructions.
 - i) Logic instruction
 - ii) Data transfer instruction
 - iii) Bit-oriented instruction. (6mks)
 - b) Discuss the following types of operations.
 - i) Arithmetic
 - ii) System control
 - iii) Conversion. (6mks)
 - c) Explain the following micro-operations.
 - i) Fetch cycle
 - ii) Indirect cycle. (4mks)

- d) Differentiate between a linear and non-linear pipeline.(4mks)
 - e) Explain the registers found in the register window. (4mks)
 - f) Discuss the following terms as used in RISCs. (6mks)
 - i) Procedure calls
 - ii) Operation
- 2.
- a) Using an example describe the following logical operations.
 - i) Logical shift
 - ii) Rotate shift (6mks)
 - b) Differentiate between a hardwired implementation and a micro programmed implementation of a control unit? (4mks)
 - c) i) Briefly explain the two basic approaches used to minimize register-memory operations on RISC machines. (6mks)
 - ii) What are some typical characteristics of a RISC instruction set architecture? (4mks)
- 3.
- a) Using a diagram describe the fetch, indirect, execute and instruction cycle as used in micro-operations.(10mks)
 - b) i) Explain the register organization of a computer system. (5mks)
 - ii) Explain the two categories of pipeline processing. (5mks)
- 4.
- a) Describe the processor organization of a computer system.(6mks)
 - b) i) Describe the concept of instruction pipelining. (4mks)
 - ii) Using a diagram explain the 5 basic stages of pipelining in RISC machine. (10mks)
- 5.
- a) Using a diagram discuss the instruction cycle states.(14mks)
 - b) Discuss three interrupts in the instruction cycle. (6mks)