MACHAKOS UNIVERSITY

University Examinations 2016/2017

SCHOOL OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

FIFTH YEAR FIRST SEMESTER EXAMINATIONS FOR BACHELOR OF SCIENCE IN ELECTRICAL AND ELECTRONICS ENGINEERING

EEE 556: PROGRAMMABLE LOGIC CONTROLLERS

DATE: 24th JULY 2017 **TIME: 8:30 – 10:30 AM**

ANSWER QUESTION 1 AND ANY OTHER TWO

QUESTION ONE (COMPULSORY) (30 MARKS)

a) What is a programmable logic controller? (3 marks)

b) Programmable controllers offer several advantages over a conventional relay type of control. List and explain these advantages. (7 marks)

c) With the help of a well labelled diagram, describe the architecture of the PLC system. (7 marks)

d) State and explain two PLC disadvantages. (2 marks)

e) The basic PLC scan cycle consists of three steps. State and explain these steps. (6 marks)

f) There are three machines, each with its own start and stop buttons. Any two machines may run at one time (also, any one may run by itself). Each start button is to have a sealing circuit. Construct a PLC circuit with appropriate interlocking for this problem. (5 marks)

QUESTION TWO (20 MARKS)

a) Describe the differences between an [XIC] and an [OSR] instruction. (4 marks)

b) A certain switch (I:1/0) is to start a process. The process is to run for 30 seconds, stop for 10 seconds and then repeat as long switch I:1/0 remains closed. Opening I:1/0 at any time is to reset all timers and de-energize all outputs. Output O:2/0 is to be energized during the 30s run period and output O:2/1 is to be energized during the 10s stop period. During the run period, a single output O:2/2 is controlled by input I:1/1. If I:1/1 is open (at the beginning of the run period) O:2/2 is to be off for the first 5 seconds then on for 10 seconds. If I:1/1 is closed (at the beginning of the run period) O:2/2 is to be off for the first 10 seconds then on for 15 seconds. Changing I:1/1 after the run period has begun should not change the above sequence. Output O:2/2 is always to be off during the stop period. Construct the PLC circuit that realises the above operation. (8 marks)

c) Show how basic AB PLC addressing is done. (5 marks)

d) Describe the output energize (OTE) instruction. (3 marks)

QUESTION THREE (20 MARKS)

a) Using appropriate ladder logic illustrations, describe the following Boolean statements: Logical AND, Logical OR and Logical NOT. (6 marks)

b) Describe PLC retentive and delay timer functions. (4 marks)

c) List and describe four PLC timing functions that are commonly used in circuits and rocesses. (4 marks)

d) Construct a PLC timing circuit that will output (using output O:2/0) a 0.5 second pulse every two seconds (i.e. on for 0.5s then off for 2s) if a switch (using I:1/0) is closed and a 1 second pulse every two seconds if the switch is open. (6 marks)

QUESTION FOUR (20 MARKS)

a) Describe the Up Counter (CTU) instruction **(**4 marks)

b) A certain process is to count the number of true-to-false transitions on input **I:0.0/0** for a 10 second period. Counting is to occur if input word **I:0.1** has a value less than 10000 or greater than 20000. The 10 second counting period is to begin 15 seconds after the process starts. **I:0.0/1** is a process start input and input **I:0.0/2** is a process stop input. The count display is to be output to word **O:0.0** only at the end of the count period. All outputs are to be de-energized 5 seconds after the count period. The process should repeat only after another distinct press of the process start input. Write an efficient ladder logic program for this process. (8 marks)

c) Write a program that ANDs **B3:0** with **B3:1** when **I:0.0/0** is energized, ORs **B3:0** with **B3:1** when **I:0.0/1** is energized, XORs **B3:0** with **B3:1** when **I:0.0/2** is energized and COMPLEMENTS **B3:0** when **I:0.0/3** is energized. **B3:1** is to hold the result in each case. If more than one input **I:0.0/0-I:0.0/3** is energized, only one of the operations will be performed. The precedence order for operations should be from AND (highest precedence) to COMPLEMENT (lowest precedence). (8 marks)

QUESTION FIVE (20 MARKS)

a) Discuss the setup and use of subroutines within the Allen Bradley PLCs. (5 marks)

b) Assume there are sixteen stations along a conveyor system. The stations are numbered from 0-15 with station zero being the first (*i.e.* the point where parts enter the conveyor). Parts are to advance along the conveyor at the rate of one station every four seconds. A part may or may not be at a given station at any point in time. An input sensor **I:0.0/0** is used to detect a part entering the conveyor. At station 5, parts are checked for defects and an input sensor **I:0.0/1** is energized if the part is defective. At station 10, any defective parts are to be removed from the conveyor by energizing output **O:0.0/0**. Write an efficient ladder logic program for this process. (6 marks)

c) Design an efficient ladder logic program that samples analog input (I:1.0) at the rate of 2Hz and outputs the average value to analog output O:1.0 once every two seconds. (6 marks)

d) Show a diagram of a typical input for a current sinking input module. (3 marks)