MACHAKOS UNIVERSITY

SUPPLEMENTARY EXAM

SIT 112: INTRODUCTION TO DIGITAL ELECTRONICS

DATE: AUGUST 2018 DURATION: 2 HOURS

Instructions: Answer questions ONE and ANY other TWO questions.

QUESTION 1

i. All the number system used in digital electronics have positional value notation. Explain the meaning of positional value basing your argument on decimal number system. (1 mark)

ii. Convert the binary number 11001_2 into its octal form (2 marks)

iii. Convert $23A_{16}$ into its decimal equivalent (1 mark)

b) Perform the following binary operations (3 marks)

i) Add 110011_2 to 101101_2

ii) Subtract 01011_2 from 10110_2

iii) Multiply 111_2 by 101_2

c) i) Write 9 and 14 in excess -3 code (1 mark)

Information interchanges (2 marks)

d) i) Explain briefly using a simple block (logic) diagram of a simple digital system how human language is converted into machine language and vice versa (2 marks)

ii) Construct the truth table of 3-input ORgate with inputs A B C and output D(2 marks)

e) i) Carry out the binary division $11011_2 \div 100_2$(1 mark)

ii) Find the equivalent decimal value for the BVD coded number 0001010001110101(2 marks)

f) i) Construct the truth table of an Half-adder (1 mark)

ii) Define the following terms Flip-flop; register (1 mark)

iii) Draw a logic diagram of a mod-8 ripple counter using three JK flip-flops (2 marks)

g) i) Prove the following Boolean identity (A+B) (A+C)=A+BC(2 marks)

ii) Simplify the Boolean expression y=ABCD+ABCD+BCD show the minimum gate implementation (3 marks)

h) i)Design a logic hardware based on Boolean expression AB+C (2 marks)

ii) Find the canonical sum of products (SOP) form the expression f (A B C D) =AB+AC+A.C (2 marks)

Q2. a) With the help of a logic circuit of a half-adder using NOR gates show how the sum(s) and carry (C) operations are carried out. (5 marks)

b) Differentiate between the following terms as used in logic circuits of digital systems.

i) Synchronous sequential circuits and asynchronous sequential circuits (2 marks)

ii) Multiplexers and demultipexers (2 marks)

c) i) Construct the reset-set flip-flop using two cross coupled NAND gates(3 marks)

ii) Draw the logic circuit diagram of four stage lift shift left register with D-flops (4 marks)

d) Construct the table showing the counting sequence for a 4 bit (mod-16) serial counter (4 marks)

Q3 a) Perform the following Boolean operations (4 marks)

i)1011.01+1001.11

ii) 110.01-100.10

Iii) 101.00x11

IV) 11.11÷0.101

b) Convert the following numbers to their respective forms

i) Decimal 1996 to an equivalent binary number (1 mark)

ii) Octal 3711 to its decimal form(2 marks)

iii) Hexadecimal CD42 to its binary and decimal systems (3 marks)

c) Subtract

i) $(1011101)_2$-$(1101100)_2$ using the I's complementary method (1 mark)

ii)$(1010)_2$-$(1101)_2$ using the 2's complementary method (2 marks)

d) i) Express 493 in 8421 code 2421 code 5211code and $84\bar{2}1$ code (4 marks)

ii) A seven bit Hamming code is received as 1101101. Locate the error position and give the correct code (3 marks)

Q4 a) i) define the term logic gate as used in digital circuits (1 mark)

ii) The AND gate represents a logical Boolean multiplication. Draw the logic symbol for a 3-input AND gate. Give its equivalent switching circuit and construct the corresponding truth table (4 marks)

b) i) The NOR gate is a universal gate. Draw the logic symbol of a NOR gate .Explain how it is used as an AND gate and draw the gate implementation diagram(3 marks)

ii) Construct the truth table for a 2-input NAND gate and explain the NAND gates operations as compared to the NAND gates (2 marks)

c) Prove the following identities using Boolean expressions (3 marks)

i)$\overline{AB+BC+CA}=\overline{A}\overline{B}+\overline{B}\overline{C}+\overline{A}\overline{C}$

II) $\overline{\overline{A}\overline{B}+\overline{A}+AB}=0$

d) i)Design the logic circuit whose output is given by the Boolean expression D=(A+B).C

Evaluate D when A=O B=1 C=1 and when A=1 B=1 C=0(3 marks)

ii)Design the logic circuit using NAND gates only to implement the following Boolean expression Y=ABC+DEF(4 marks)

Q5 a) i) Differentiate between min terms and max terms as used in Karnaugh map method of Boolean expression simplification (2 marks)

ii) Find the sum of minterms and function f(ABCD)in conocal sum of products form for the function f(ABCD)=A.C (4marks)

b) Obtain the minimal expression for the Boolean switching function given below using the Karnaugh map method f(WXYZ)=∑(0123489 10 15)(5 marks)

c) From the truth table below find the max terns or conical POS form of function f(A B C) (5 marks)

A	B	C	D
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1

1	0	1	0
1	1	0	0
1	1	1	1

d) Construct the truth table for a binary full-adder which adds three bits of binary data producing a sum bit S and a final carry bit C (4 mark)