MACHAKOS UNIVERSITY

ISO 9001:2008 Certified

University Examination for 2015/2016

SCHOOL OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
THIRD YEAR SUPPLEMENTARY EXAMINATION FOR BACHELOR OF SCIENCE IN ELECTRICAL AND ELECTRONICS ENGINEERING

EEE 305: DIGITAL ELECTRONICS I

DATE: __2017_____ **TIME: 2 HRS**

INSTRUCTIONS.

Answer **QUESTION ONE** and **any other TWO.**

Do **NOT** answer **MORE** than **three** questions.

QUESTION ONE (30 MARKS)

(a) What is a universal gate? Give examples. Realize the basic gates (AND, OR, NOT gates) with NAND gate. (8mks)

(b) When simplified with Boolean Algebra (x + y)(x + z) simplifies to? (3mks)

(c) What is the decimal equivalent of Binary number 110101101? (2mk)

(d) For the function below, write the truth table, then simplify using Karnaugh map and realize the function using NAND gates only. $F = A.B.C + B.C.\overline{D} + \overline{A}.B.C$ (7mks)

(e) Convert the octal number 7401 to Binary. (3mks)

(f) With the help of a suitable diagram, explain how you convert a JK flip flop to T type flip flop. Also draw the excitation tables of both flip flops. (7mks)

QUESTION TWO (20 MARKS)

(a) Find the Boolean expression for logic circuit shown in Fig.1 below and reduce it using Boolean algebra. (5mks)

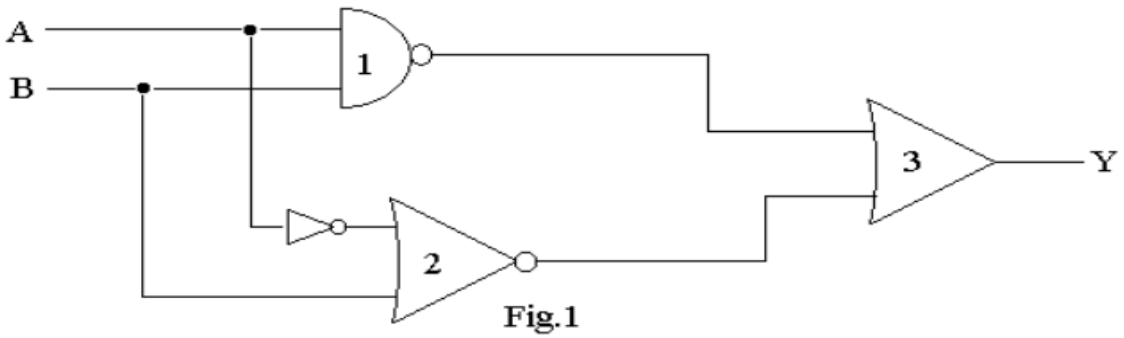


Fig.1

(b) Perform 2's complement subtraction of the following: $(7)_{10} - (11)_{10}$ (3mks)

(c) Draw the circuit diagram of a Master-slave J-K flip-flop using NAND gates. What is race around condition? How is it eliminated in a Master-slave J-K flip-flop? (5mks)

(d) Simplify the following expression into sum of products using Karnaugh map:

$$F(A,B,C,D) = \sum (1,3,4,5,6,7,9,12,13)$$ (7mks)

QUESTION THREE (20 MARKS)

(a) Simplify using Boolean algebra and draw the combinational logic diagram for the given expression:

$$F = \overline{ABC} + \overline{AB}C + \overline{A}B\overline{C} + A\overline{BC} + A\overline{B}C$$ (7mks)

(b) Distinguish between combinational logic circuits and sequential logic circuits. How are the design requirements of combinational circuits specified? (4mks)

(c) Distinguish between min terms and max terms. (3mks)

(d) Prove the following Boolean identities using the laws of Boolean algebra: (6mks)

(i) $(A+B)(A+C) = A + BC$

(ii) $ABC + A\overline{B}C + AB\overline{C} = A(B+C)$

QUESTION FOUR (20 MARKS)

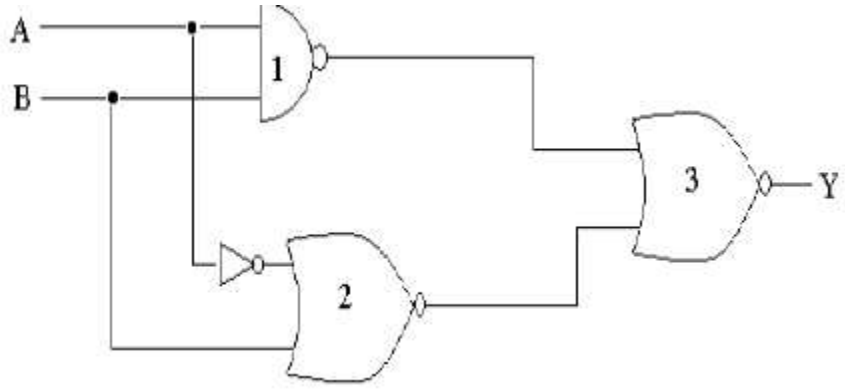
(a) Perform the following operations using the 2's complement method: (7mks)

(i) $23 - 48$ (ii) $-48 - 23$

(b) The Karnaugh map for a SOP function is given below in Fig below. Determine the simplified SOP Boolean expression. (4mks)

AB \ CD	00	01	11	10
00	1	1		1
01		1		
11				
10	1	1		1

(c) Find the reduced Boolean expression for the logic circuit shown below using Boolean algebra . (4mks)



(d) Reduce the following equation using k-map. (5mks)

$$Y = B\overline{C}\,\overline{D} + \overline{A}\,B\,\overline{C}D + A\,B\,\overline{C}D + \overline{A}\,B\,C\,D + A\,B\,C\,D$$

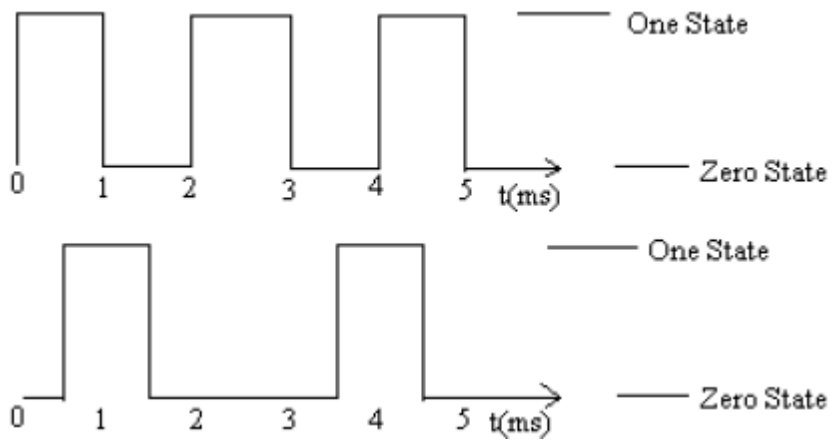
QUESTION FIVE (20 MARKS)

(a) What is a flip-flop? What is the difference between a latch and a flip-flop? List out the application of flip-flop. (4mks)

(b) Give the truth table of S-R and D-flip flops. Convert the given S-R flip flop to a D-flip flop. (5mks)

(c) The voltage waveforms shown in Fig. below are applied at the inputs of 2-input AND and OR gates.

Determine the output waveforms for each. (6mks)



(d) What are the advantages of CMOS logic? Explain CMOS Inverter with the help of a neat circuit diagram. (5mks)