MACHAKOS UNIVERSITY

University Examinations for 2016/2017

SCHOOL OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

THIRD YEAR SECOND SEMESTER EXAMINATION FOR BACHELOR OF SCIENCE IN MECHANICAL ENGINEERING

EMM 300: ENGINEERING ELECTRONICS

DATE: 20/6/ 2017 **TIME:8.30-10.30 AM**

Instructions

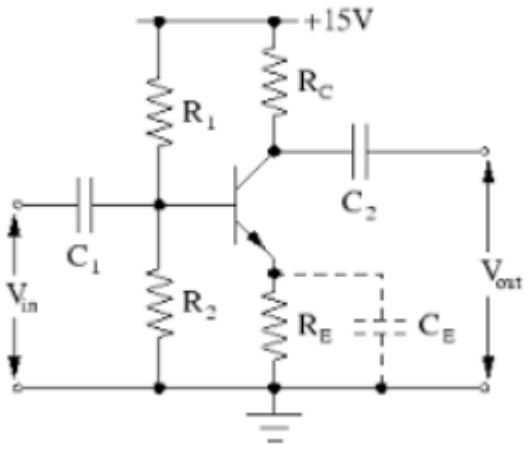
- *This paper consists of Five Questions*
- *Attempt* ***Question One*** *(Compusory) and any other* ***Two Questions***

QUESTION ONE

a) From the definitions of α and β, Show that (6 marks)

$$I_C = \frac{\alpha}{1-\alpha} I_B = \frac{\beta}{1+\beta} I_E$$

b) The diagram in Fig Q. 1b) shows a CE Amplifier with a Voltage Divider Bias. From the first principles derive the respective currents in the BJT and Voltage across the emitter in terms of the circuit parameters (5 marks)



c) The diagram in Fig Q. 1c) shows a Voltage Divider Bias. From the first principles determine

i. Emitter current

ii. Collector current

iii. Voltage across the collector and emitter (6 marks)

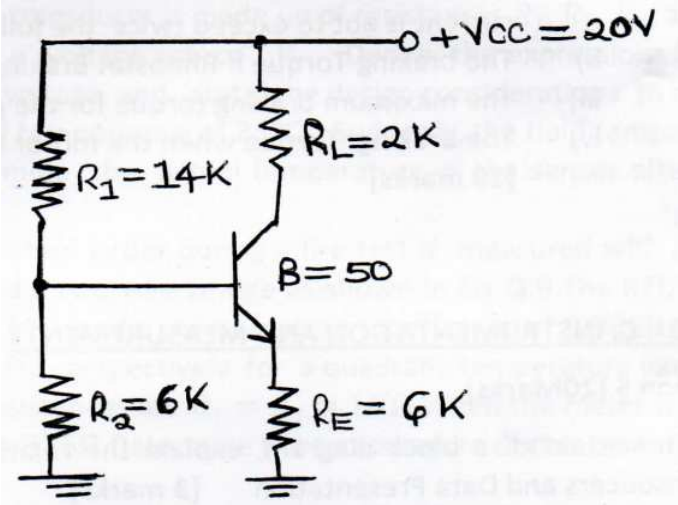


Fig Q.1b)

d) The CE amplifier shown in the Fig Q.1d employs an emitter feedback. Determine the change in the dB power gain if the emitter bypass capacitor is removed ,giving reasons in each case.Take β=100 , $r_{e=25mV/I_E}$(and ignore V_{BE} (8 marks)

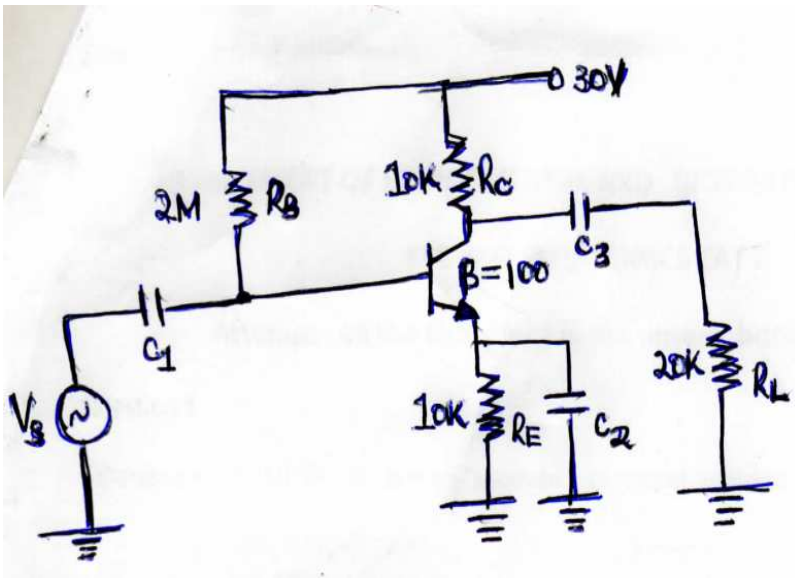


Fig Q. 1c)

e) For the logic network in Fig Q 1 e) ;

i. Determine the logic expression

ii. Produce the truth table

iii. Express the logic expression in 3 a) above as a sum of product (SOP) in its simplest form (5 marks)

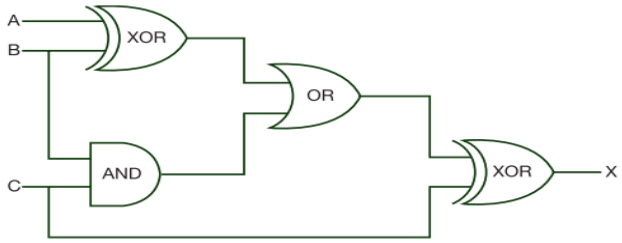


Figure Q.3

QUESTION TWO

The basic **RC Oscillator** which is also known as a **Phase-shift Oscillator,** produces a sine wave output signal using regenerative feedback obtained from the resistor-capacitor combination. OP-AMP based RC oscillator is as shown in Figure 2.0 as shown

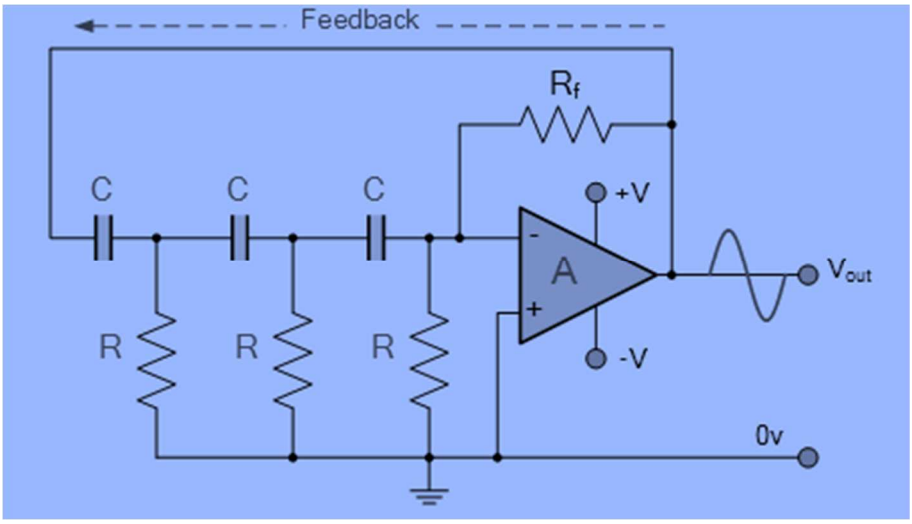


Figure 2.0: OP-AMP Based RC Oscillator

a) If all the resistors, R and the capacitors, C in the phase shift network are equal in value, then show that for sustained oscillation,

i. The amplifier gain must be 29 and inverting (9 marks)

ii. The frequency of oscillations produced by the RC oscillator is given as

$$f_0 = \frac{1}{2\pi RC\sqrt{2n}}$$

where is n the number of RC stages (2 marks)

b) If the OP-AMP is replaced by a BJT then show that (10 marks)

$$h_{fe} = -(23 + 4k + \frac{29}{k})$$

c) Other than the RC oscillator state other *Four Types* of Oscillators (4 marks)

QUESTION THREE

A single phase transformer with secondary voltage of 230V 50HZ delivers power to a load $R = 10\ \Omega$ through a half wave controlled rectifier circuit. For a firing angle delay of 60^0,

a) Sketch a well labeled diagram of the Rectifier Circuit plus transformer (2 marks)

b) Determine from the *First Principles*

i. Average voltage current and DC power (4 marks)

ii. Rms output voltage, current and AC power (4 marks)

iii. Rectification efficiency (2 marks)

iv. Form factor (2 marks)

v. Voltage ripple factor (2 marks)

vi. Transformer utilization factor (2 marks)

vii. PIV of the thyristor (2 marks)

QUESTION FOUR

a) Convert the Decimal fraction 0.426 to Binary fraction (1 mark)

b) Convert the Binary fraction 10110.101 to decimal fraction (1 mark)

c) Convert 2543 BCD to Binary (1 mark)

d) Using 1s and 2s complement, determine 7-22 (2 marks)

e) Perform $112_{10} + 65_{10}$ using the 2s complement arithmetic (2 marks)

f) Convert 7325_8 to Binary (1 mark)

g) Convert the decimal to 750 HD (1 mark)

h) Perform the HD computation $B7H - 4DH$ (1 mark)

i) In TTL logic,four three-input logic gates are involved.The HIGH State is fed from a 4V supply and the low state is at 0.4V,ideally zero. A change in state occurs in 20ms at a current of 10mA.Determine for the TTL

i. Logic levels
ii. Fan in
iii. Fan out
iv. Noise margin
v. Propagation delay
vi. Power dissipation(PD)
vii. Speed power product(SPP) (6 marks)

j) Design and Sketch an OP-AMP circuit that will produce an output equal to $V_0 = -(4V_1 + V_2 + 0.1V_3 + 10V_4)$.Assume that the feedback path has a resistance of $100K\Omega$ (4 marks)

QUESTION FIVE

a) Using *Logic Circuits,* discuss the universality of gates and compare them with the bubbled gates (5 marks)

b) Using Demorgan's Theorem, prove that the coincidence gate provides the inverse function to an or gate (4 marks)

c) A manufacturing process is controlled by a built in logic circuit which is made up of AND, OR and NOT gates only. The process receives a STOP signal (i.e. X = 1) depending on certain conditions, shown in Table Q.5:

INPUTS	BINARY VALUES	CONDITION IN PROCESS
V	1	Volume > 1000 litres
	0	Volume <= 1000 litres
T	1	Temperature > 750°C
	0	Temperature <= 750°C
S	1	Speed > 15 metres/second (m/s)
	0	Speed <= 15 metres/ second (m/s)

Table Q.5

A stop signal (X = 1) occurs when: either Volume, V > 1000 litres and Speed, S <= 15 m/s or Temperature, T <= 750ºC and Speed, S > 15 m/s.The output consists of the all the possible situations when the stop signal could be received

i. Derive the logic expression

ii. Draw the logic circuit

iii. Draw the truth table (6 marks)

d) An electrical motor is to operate when :(i)The power supply (P) is connected (ii)The current taken from the supply is less than the safety figure(I) (iii)The power supply should not be able to be switched on unless a safety guard (S) is in position ,although this can be overridden by a maintenance technician by means of a special key(K). Implement the motor using XOR Gate and AND Gate (5 marks)